

# Transmission electron microscopy observation of CMOS devices of titanium self-aligned silicide technology with nitrogen ( $N^+$ ) implantation process

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TiSi<sub>2</sub> is widely used as contact, gate and interconnect material in high-performance metal-oxide-semiconductor (MOS) devices because of its low resistivity (15–20  $\mu\Omega\text{-cm}$ ) [1], high-temperature stability and “self-aligned” properties [2, 3]. The rapid scaling in device dimensions necessitates the use of low resistivity materials for interconnects and also for back-end metallization. The implementation of the Ti self-aligned silicide (SALICIDE) process becomes increasingly difficult, however, especially at the deep sub-micron regime as a result of the well-known “fine-line effect” [4, 5]. Hiroshi [6] reported that low-leakage and low-resistance sub-micron silicided complimentary metal oxide semiconductor (CMOS) devices are achievable through Ti SALICIDE technology with recoil nitrogen ions, which were introduced through a contamination-restrained, oxygen-free, low-pressure, chemical-vapor-deposited nitride layer. In this work, we directly implanted nitrogen ion ( $N^+$ ) to understand the bulk effects of deeply implanted nitrogen. Cross-sectional transmission electron microscopy (XTEM) analysis was performed to investigate the changes associated with  $N^+$  implantation in the Ti SALICIDE process and to relate these changes to the electrical properties observed.

In this experiment, a *p*-type (100)-oriented silicon wafer was used as the substrate for device fabrication. Nitrogen ions ( $N^+$ ) with  $5 \times 10^{15}$  ions  $\text{cm}^{-2}$  dosage and 80 keV energy were introduced through ion implantation. The projected range ( $R_p$ ) of the  $N^+$  implantation was about 0.2  $\mu\text{m}$  based on transport of ions in matter (TRIM) 90 simulations. Subsequently, a single layer of 70 nm Ti was deposited by physical vapor deposition (PVD) followed by a first rapid thermal anneal (RTA) at 690 °C and second RTA at 850 °C to form the final C-54 phase TiSi<sub>2</sub> film.

Fig. 1 is a XTEM image of the control specimen, i.e., without  $N^+$  ion implantation. The thickness of the C-54 TiSi<sub>2</sub> film is about 91 nm. No significant defects were observed in this specimen. For the  $N^+$ -implanted specimen, we observed (1) a thicker C-54 phase TiSi<sub>2</sub> film on the narrow poly-Si gate, (2) defects near the spacer and field oxide and (3) two layers of end-of-range (EOR) defect in the under-

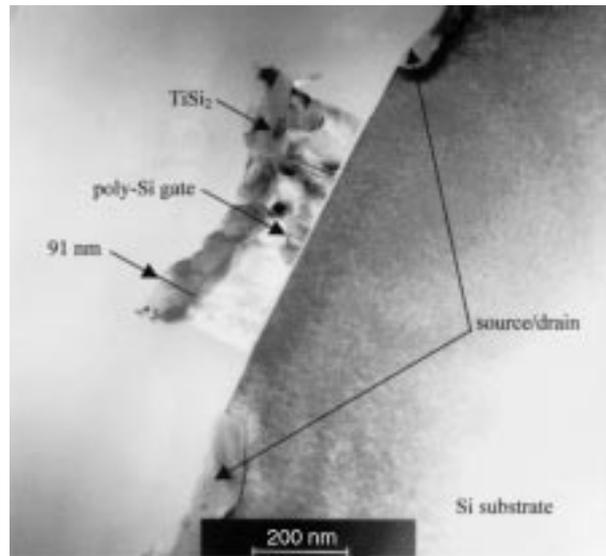
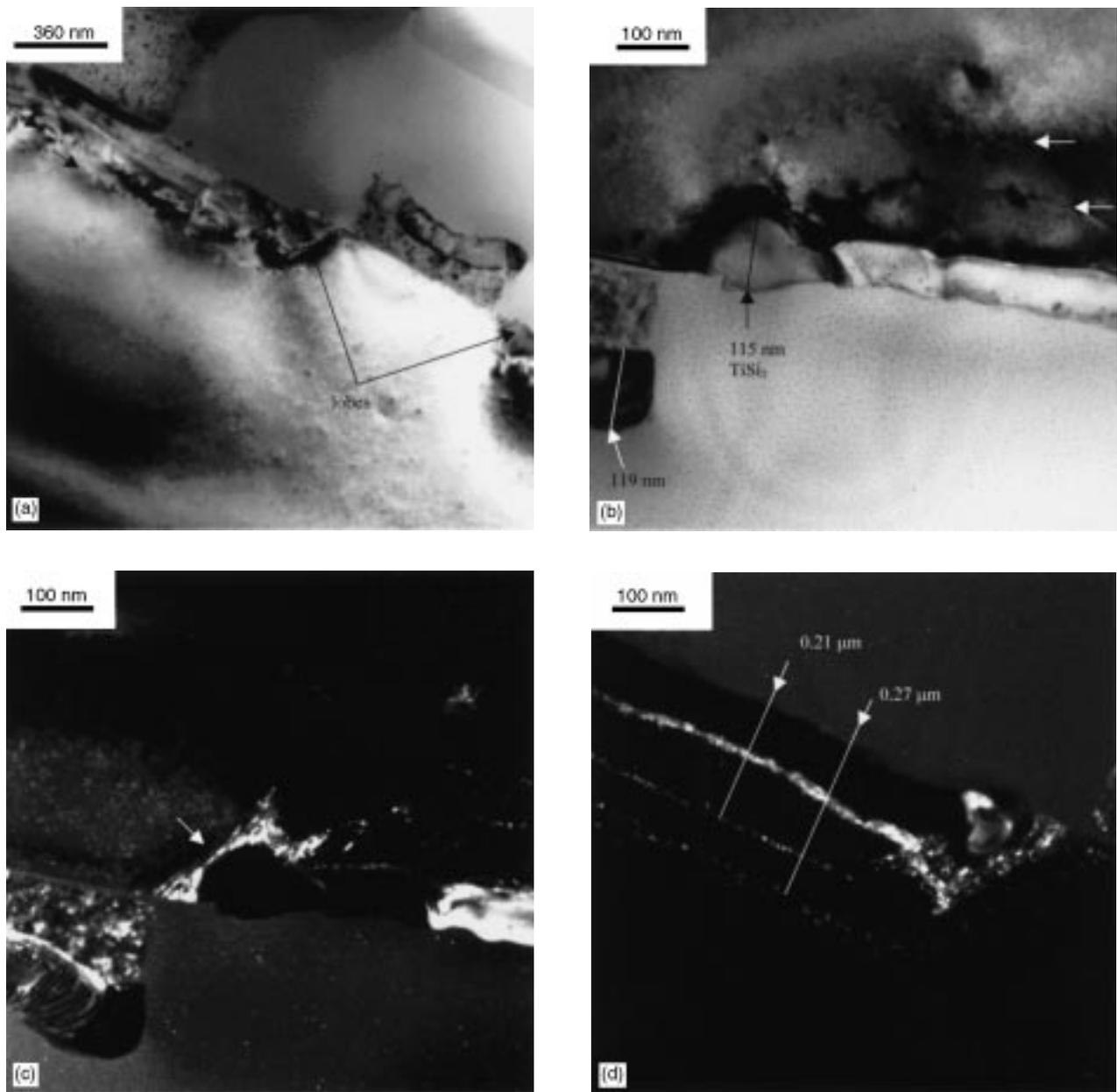


Figure 1 Bright-field XTEM image of reference specimen (without  $N^+$  implantation). The C-54 TiSi<sub>2</sub> film is measured to be 91 nm on top of narrow poly-Si gate.

lying Si substrate. All these observed abnormalities are likely to influence the device performance.

1. A thicker C-54 phase TiSi<sub>2</sub> film can be observed after  $N^+$  implantation in Fig. 2a and b. The thickness of the C-54 TiSi<sub>2</sub> phase film was measured to be 119 nm. We attribute this observation to enhanced diffusion of Si due to the damage induced by the  $N^+$  implantation. This increase in TiSi<sub>2</sub> thickness serves as an explanation for the lower sheet resistance measured on narrow poly-Si gates after incorporation of  $N^+$  ions.

2. Defect structures were observed in the Si substrate after  $N^+$  implantation. First, a lobe-shaped growth can be observed at the extremities of the source/drain close to the oxide spacer, and this was a general feature of these contacts in this specimen. It can be seen in Fig. 2b that the lobe has extended underneath the oxide spacer. The growth of the TiSi<sub>2</sub> lobe is attributed to the increase in  $N^+$  ion concentration near the spacer region due to deflection of  $N^+$  ions by the spacer (see Fig. 3), causing an increase in TiSi<sub>2</sub> growth. The formation of the



*Figure 2* (a) Bright-field XTEM image of typical  $N^+$  implanted specimen with poly-Si gate and source/drain region.  $TiSi_2$  lobes and two layers of defects (arrow) were shown in source/drain junction region. (b) A high-magnification bright-field image of the same specimen showing a thicker  $TiSi_2$  film (119 nm) on the narrow poly-Si gate. A  $TiSi_2$  lobe 115 nm thick was observed at the source/drain region near the oxide spacer beside two layers of EOR defects formed in the Si substrate. (c) Weak-beam,  $g = (400), 3g$ , image of the same specimen showing dense parallel-line defects in the Si substrate near the spacer and active field oxide. (d) Weak-beam  $g = (111), 3g$ , image of the same specimen showing two EOR defect layers (at  $0.21 \mu m$  and  $0.27 \mu m$  from original Si surface).

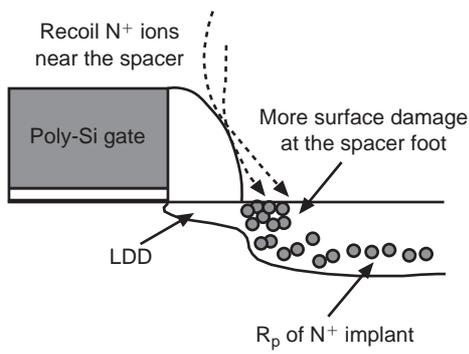
$TiSi_2$  lobe appears to have a secondary effect in generating other defects, including dislocations. These defects were evident in the weak-beam XTEM image (Fig. 2c), and they indicate regions of increased mechanical or thermal stress due to the abnormal lobe growth phenomena. The defects in this critical region, i.e., in the region between the source/drain and the gate, should be expected to cause severe leakage currents.

3. Likewise, two layers of EOR defects were observed, as shown in Fig. 2d. This weak-beam image shows that one layer of EOR defects extends from the field oxide isolation into the Si substrate (to a depth of  $0.27 \mu m$  from the Si surface), while the other layer extends from the  $TiSi_2/Si$  interface to a depth of  $0.21 \mu m$ . It was noticed that these defects

only occur after  $N^+$  implantation. They could result from clusters of point defects [7] or from precipitation of a dopant-related compound, such as boron nitride (BN), or from dislocations due to a high concentration of interstitial  $N^+$  ions. The EOR defect layers may be expected to increase leakage across the source/drain junction to the Si substrate.

The use of  $N^+$  implantation in the Ti SALICIDE process was found to reduce the sheet resistance on narrow poly-Si gates and also on the  $n^+$  active diffusion region. The electrical sheet resistance measurement in Fig. 4a shows that the sheet resistance of the  $n^+$  poly-Si gate is reduced to  $1.7\text{--}2.5 \text{ ohm sq}^{-1}$ , which is lower than that of the reference wafer ( $2\text{--}4 \text{ ohm sq}^{-1}$ ). Fig. 4b shows that

**During N<sup>+</sup> Implantation:**



**After TiSi<sub>2</sub> Formation:**

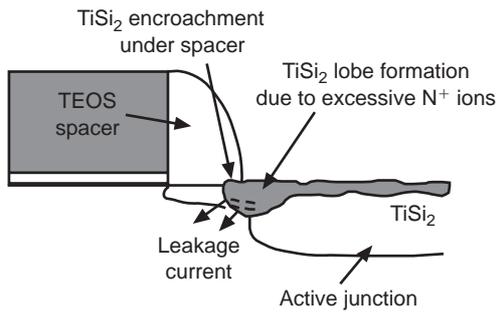
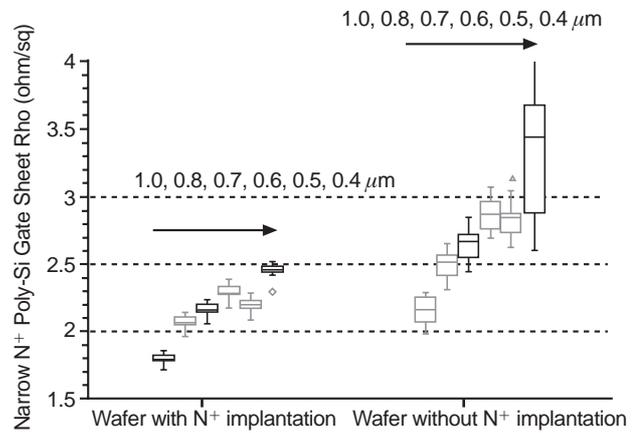
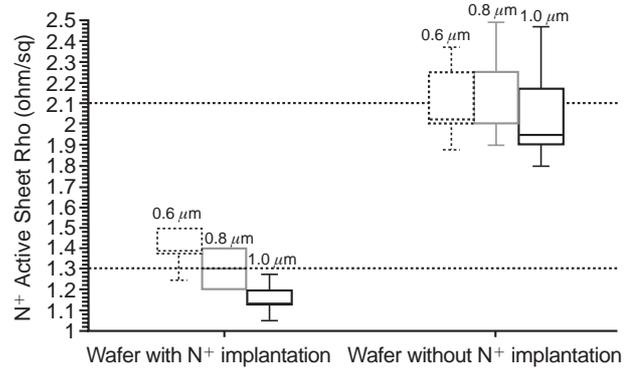


Figure 3 As a result of the surface topography during N<sup>+</sup> implantation, recoil N<sup>+</sup> ions (dotted line) cause increased surface damage and a higher N<sup>+</sup> ion concentration near the spacer region. After TiSi<sub>2</sub> formation, lobes form.

the n<sup>+</sup> active sheet resistance ranges from 1.04–1.5 ohm sq<sup>-1</sup>. Again, it is lower than that of the reference wafer (1.8–2.5 ohm sq<sup>-1</sup>), which is similar to Hiroshi's result. The observed defects in the Si substrate, however, will result in a higher junction leakage and gate-to-source/drain leakage. As illustrated in Fig. 5a, the gate-to-source/drain leakage is at least 300 times higher in the nitrogen-implanted sample than in the reference wafer. Fig. 5b shows that junction leakage for the p<sup>+</sup>/n well is over 1000 times higher than in the reference wafer [8]. This conflicts with the result reported by Hiroshi. Reasons for the similarities and differences are as follows.



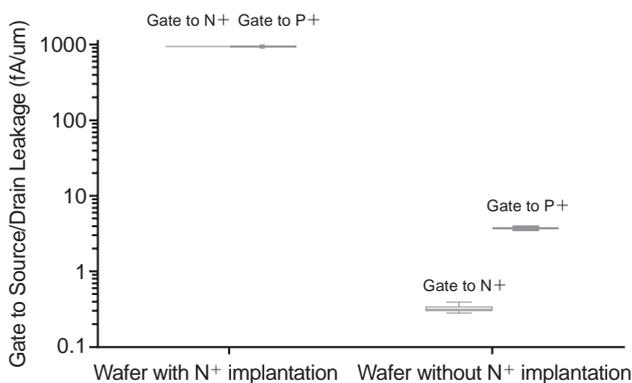
(a)



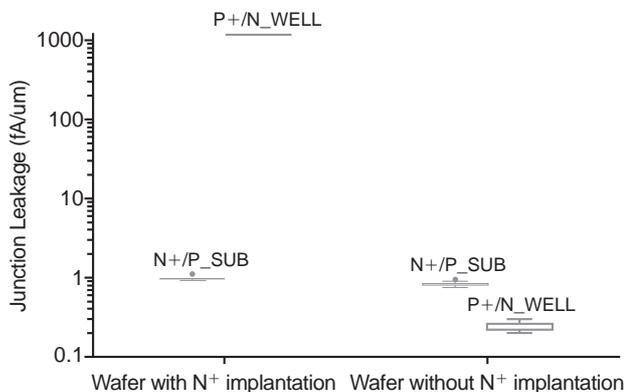
(b)

Figure 4 (a) Sheet resistance measurement of narrow n<sup>+</sup> poly-Si gate with various line widths of 1.0, 0.8, 0.7, 0.6, 0.5 and 0.4 μm. (b) Sheet resistance measurement of n<sup>+</sup> active junction with various line widths of 0.6, 0.8 and 1.0 μm.

First, a unique contamination-restrained oxygen-free Si<sub>3</sub>N<sub>4</sub> low pressure chemical vapor deposition (LPCVD) system was used by Hiroshi for Si<sub>3</sub>N<sub>4</sub> deposition. In his experiment, the nitrogen ions were introduced through p<sup>+</sup> and n<sup>+</sup> junction ion-implantation through the “contamination-free” Si<sub>3</sub>N<sub>4</sub> layer. As a result, recoil nitrogen ions were introduced into the underlying Si substrate. Thus, the reduced



(a)



(b)

Figure 5 (a) Gate-to-source/drain leakage current measurement on wafer with N<sup>+</sup> implantation compared to reference wafer without N<sup>+</sup> implantation. (b) Junction leakage current measurement on wafer with N<sup>+</sup> implantation compared to reference wafer without N<sup>+</sup> implantation.

oxygen concentration in the Si substrate may contribute to the lower TiSi<sub>2</sub> sheet resistance. In contrast, we used direct nitrogen implantation into the Si substrate to obtain low sheet resistance TiSi<sub>2</sub> as well after Ti SALICIDE.

Second, the Si<sub>3</sub>N<sub>4</sub> layer in his study inhibits oxygen diffusion during junction formation so that oxygen-related defects were reduced. Further, "it seems that the damage layer caused by ion implantation was repaired by recoil nitrogen during activation annealing before silicidation" [6]. In our experiment, the N<sup>+</sup> implantation was implemented after source/drain formation and activation annealing. Therefore, no annealing step was provided to repair the damage occurring during N<sup>+</sup> implantation before silicidation. We have found that even if the N<sup>+</sup> ion is implanted prior to p/n junction annealing (at 900 °C for 30 min) the leakage currents are also large, although reduced, showing that not all of the defects are removed.

In conclusion, we have identified several defects that occur in silicided CMOS devices with nitrogen ion-implantation after p/n junction formation. Proper controls of the N<sup>+</sup> implantation dose, energy and a separate sequence are very important in reducing defects while maintaining the low sheet resistance. An additional annealing after N<sup>+</sup> implantation might repair some of the observed defects to minimize the junction leakage currents. Further work is needed to establish this and to observe the

evolution of the defects during the annealing process.

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