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Evaluation of silicon nitride and silicon carbide as efficient polysilicon grain-growth inhibitors

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The roughness of the surface of the floating polysilicon layer in many non-volatile memory devices [1–12] has for long been critical to their electrical performance. The degree of smoothness of this polysilicon film determines the quality as well as the structural integrity of the interface that is subsequently formed with the interpoly dielectric. The occurrence of facetal grain-growth in the polysilicon film under high-temperature process conditions is the chief cause of the degradation of the film surface smoothness. Much research has been conducted to improve the surface planarity of the polysilicon surface. Tan *et al.* [2] discussed the possibility of using chemically-mechanically polished polysilicon film to replace the floating polysilicon layer. The smoothness of the film improved but the undesirable condition of facetal grain-growth, after deposition, in the polysilicon film remains probable during process steps involving oxidation or annealing [13, 14]. The substitution of a floating polysilicon layer by an amorphous silicon layer, which results in a smooth surface, has also been employed by some semiconductor manufacturers. However, amorphous films are not widely used in volume production of memory devices because of the slower deposition process and arduous control.

A process is needed that is simple to carry out and yet bears little adverse electrical and structural consequence. In this work, we introduced selected impurities to the surface of a deposited polysilicon film via low-energy ion implantation. During subsequent high-temperature process conditions, e.g. $>1000\,^{\circ}$C, the top surface of the film (≈ 30 Å) will undergo recrystallization [13]. Our purpose was that the surface impurities should act as nucleating centers and facilitate the growth of small grains near the top of the film. In this way, facetal polysilicon grain-growth should be inhibited and a smooth surface obtained.

In this experiment, a 110 Å thick tunnel oxide layer was thermally grown on a Si (110) p-typed wafer, followed by a Low Pressure Chemical Vapor Deposition (LPCVD) of a 1500 Å thick polysilicon layer (floating polysilicon). The polysilicon layer was later implant-doped with phosphorus (dose: 1×10^{15} per cm^2). The

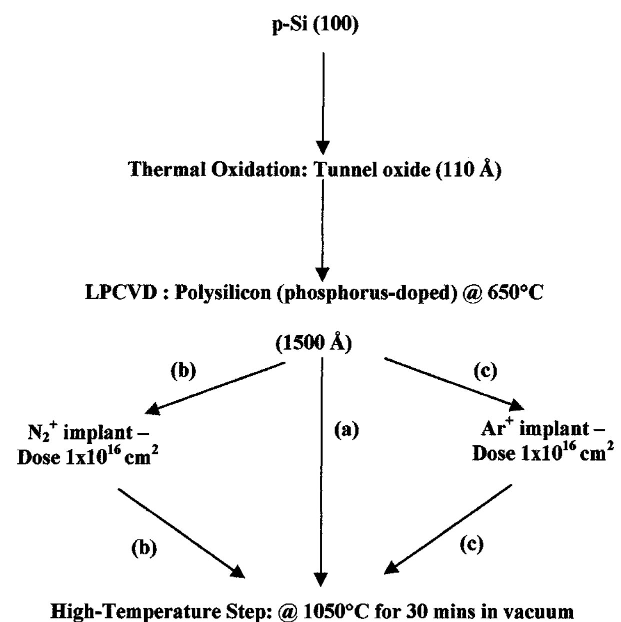

Figure 1 A block diagram showing the process steps in the formation of (a) a control specimen, (b) a N_2^+ implanted test specimen and (c) an Ar^+ implanted test specimen.

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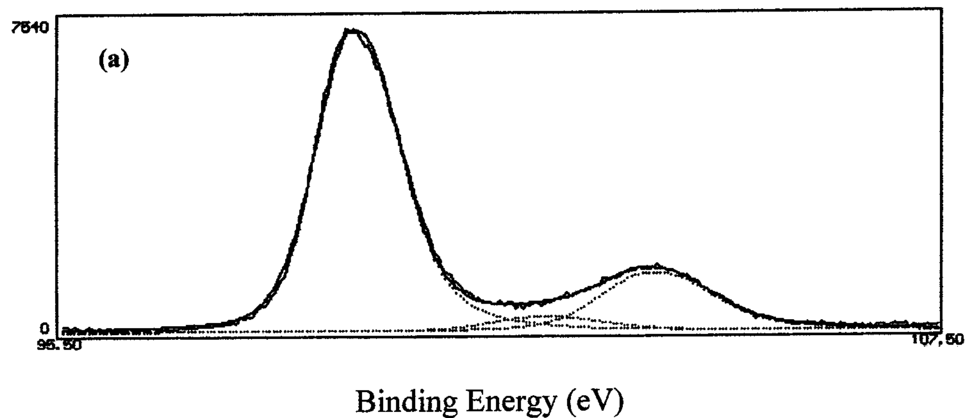

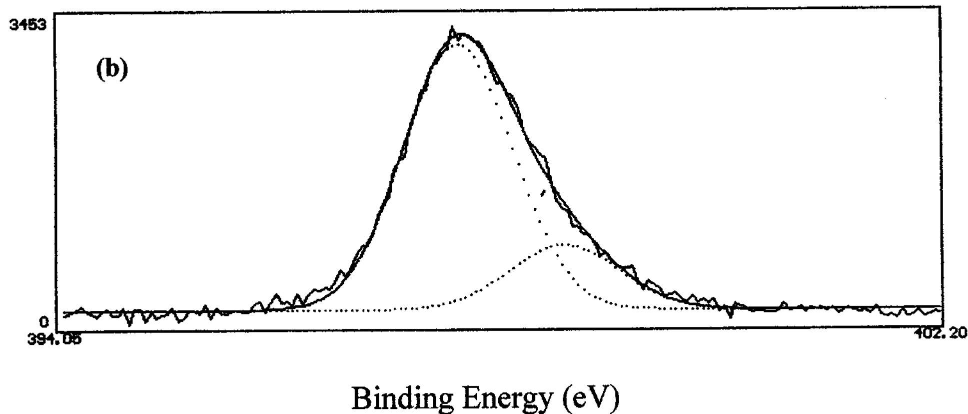

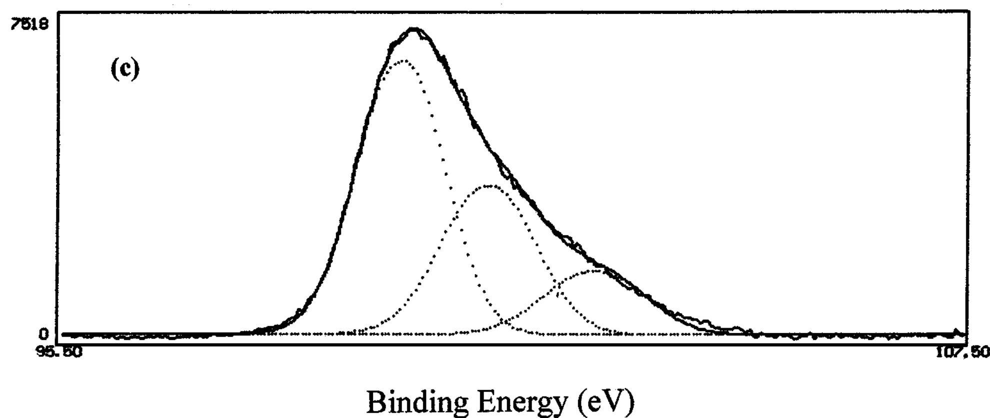

Figure 2 (a) XPS Si_{2p} core-level spectrum showing the absence of Si_3N_4 in control specimen. (Peaks (Position): Pure Si (99.4 eV); Si in Si_xO_y (102.0 eV); Si in SiO_2 (103.5 eV)); (b) XPS N_{1s} core-level spectrum showing the formation of Si_3N_4 by 2 keV N_2^+ ion bombardment in N_2^+ implanted test specimen. (Peaks (Position): N in Si_3N_4 (397.7 eV); N in N_xO_y (398.7 eV)); (c) XPS Si_{2p} core-level spectrum showing the formation of Si_3N_4 by 2 keV N_2^+ ion bombardment in N_2^+ implanted test specimen. (Peaks (Position): Pure Si (99.4 eV); Si in Si_3N_4 (100.7 eV); Si in Si_xO_y (102.0 eV)); (d) XPS C_{1s} core-level spectrum showing the absence of SiC in control specimen. (Peaks (Position): C in CH (284.5 eV); C in CO (285.8 and 287.5 eV)); (e) XPS C_{1s} core-level spectrum showing the formation of SiC by 2 keV Ar^+ ion bombardment in Ar^+ implanted test specimen. (Peaks (Position): C in SiC (283.2 eV); C in CH (284.5 eV); C in CO (285.8 and 287.5 eV)); (f) XPS Si_{2p} core-level spectrum showing the formation of SiC by 2 keV Ar^+ ion bombardment in Ar^+ implanted test specimen. (Peaks (Position): Pure Si (99.4 eV); Si in SiC (100.2 eV); Si in Si_xO_y (102.0 eV)).

wafer was then partitioned, in a clean-room laboratory, into small square pieces with side dimension of 1 cm. Some of the square specimens were then placed in an ultra-high vacuum chamber (pressure: 10^{-10} Torr) to undergo low-energy (2 keV) ion implantation. Two different ion sources were used: N_2^+ and Ar^+. SIMS analysis showed that silicon nitride (Si_xN_y: $x = 1, 1.3 < y < 1.7$) [15] and silicon carbide (SiC) respectively, are formed at the film surface. The highest concentration peaks for Si_xN_y and SiC were located at a depth around 20 and 25 Å respectively. The carbon is a contaminant in the Ar^+ implantation process. Both the N_2^+ and Ar^+ ion saturation doses were 1×10^{16} ions per cm^2 and the implantation process takes several minutes, at room temperature, to complete. Fig. 1 is a block diagram showing the process steps in the generation of (a) a control specimen, (b) a N_2^+ implanted test specimen and (c) an Ar^+ implanted test specimen.

XPS results confirmed the presence of Si_xN_y and SiC on the two implanted test specimens. Fig. 2(a) shows the XPS results of a control specimen at room temperature.

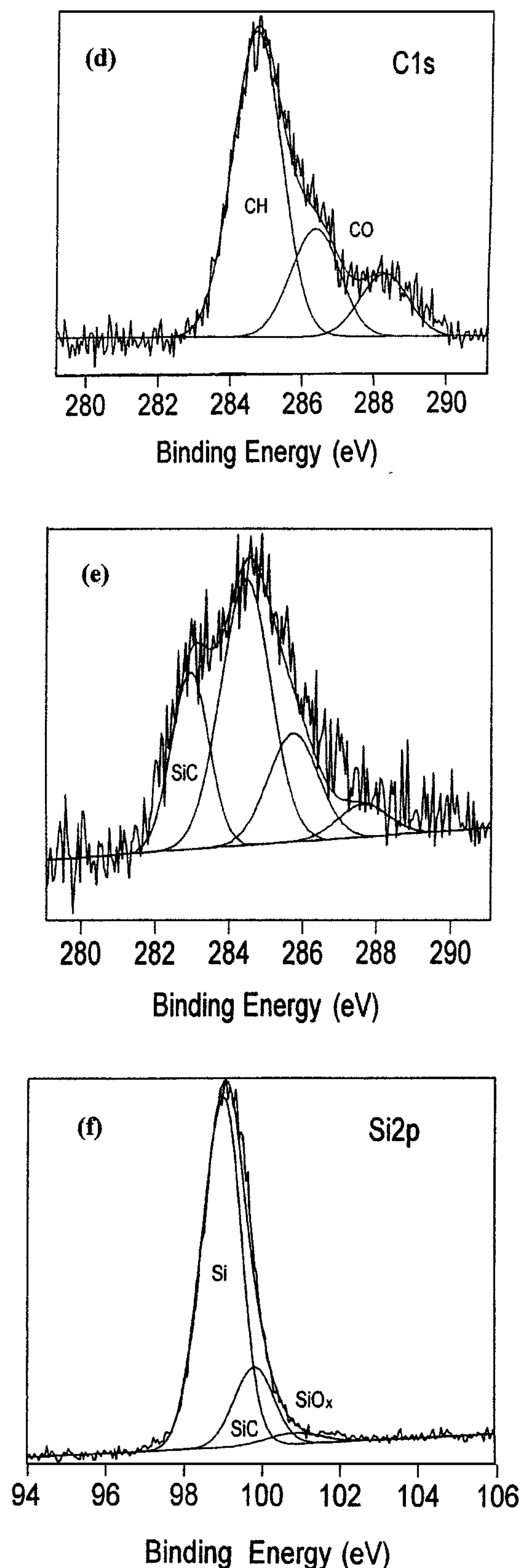

Figure 2 (Continued)

Peaks that might indicate the presence of surface Si_xN_y particles were found to be absent in the control specimen. The N_2^+ implanted test specimen, however, records XPS peaks, as in Fig. 2b and c, which indicate the presence of Si_xN_y particles. Likewise, from the Ar^+ implanted test specimen records of the XPS peaks show the presence of SiC particles (Fig. 2e and f). Such peaks were again absent in the control specimen (Fig. 2d). AFM was employed to assess the Root-Mean-Square roughness value (RMS) of both the control and test specimens. The RMS values for the various specimens were found to be similar ≈0.456 to 0.489 nm.

The control and test specimens were next placed in a vacuum furnace to undergo high-temperature treatment—1050 °C for 30 min. This step simulates the growth of a thermal oxide dielectric in the fabrication of a memory device or an annealing stage. XPS tests were again conducted on all the specimens to determine the amount of Si_xN_y and SiC that had diffused into the bulk of the polysilicon layer. Analysis of the XPS results after the high-temperature step showed that there is little reduction in the concentration of Si_xN_y and SiC particles near the top surface of the polysilicon layer. Both the diffusivities of Si_xN_y and SiC are found to be low even at high temperature. This implies that there will not be redundant Si_xN_y or SiC at locations where its presence is undesired, i.e. in the bulk of the polysilicon.

Also, the surface roughness of the control specimens and the test specimens were again assessed by AFM. The high-temperature AFM results showed results dissimilar to the earlier room temperature AFM scans. For the control specimens, the RMS value ranges from 0.550 to 0.786 nm. By contrast, the RMS values for the two types of implanted specimen range from lower values of 0.386 to 0.412 nm.

TEM specimens of the control and test specimens (after the high-temperature process step shown in Fig. 1) were then prepared by standard procedures: epoxy bonding of wafer surfaces, strengthening with electroplated copper, slicing, dimpling and ion milling at room temperature with a GATAN PIPS ion mill.

Figs 3–5 are low magnification bright-field XTEM images of the control specimen, the N_2^+ implanted test specimen and the Ar^+ implanted test specimen respectively. From the XTEM pictures, one can observe that the test specimens show a higher concentration of smaller grains in their polysilicon layer. The range of grain size in the polysilicon layer for N_2^+ implanted test specimen is from 300 to 500 Å and 200 to 400 Å for the Ar^+ implanted test specimen. In both, the grains are smaller than those in the control specimen, which show polysilicon grain sizes ranging from 1000 to 1400 Å. In the last case, the growing polysilicon grains emerging from nucleating centers located at the polysilicon/tunnel oxide interface extend as far as the film surface by the mechanism of columnar growth (Fig. 3). In the cases of both the implanted test specimens (Figs 4 and 5) nucleation has occurred at the film surface as well as at the polysilicon/tunnel oxide interface. This is related to the smaller measured grain sizes. Bearing in mind that the implantation energy is too low to cause significant amorphization at the surface, as is reflected in AFM results, the principal differences in the observed XTEM results are ascribed to the availability of the nitride and carbide.

XPS tests showed that these Si_xN_y and SiC inclusions have a much higher concentration near the surface after the high temperature anneal: there was only a minor reduction of N and C concentration at the polysilicon surface of around 10%. The concentration of nitrogen and

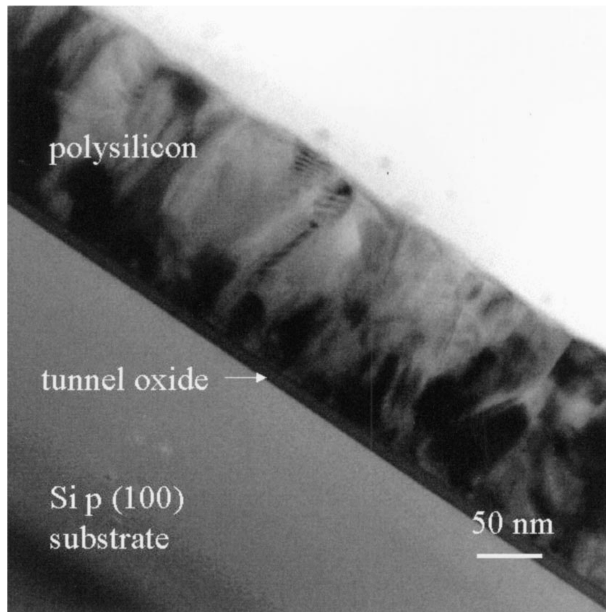

Figure 3 Low magnification bright-field XTEM picture of control specimen with 110 Å tunnel oxide and 1500 Å polysilicon on a Si p (100) substrate. Columnar grains from the polysilicon/oxide interface extending to the surface were shown.

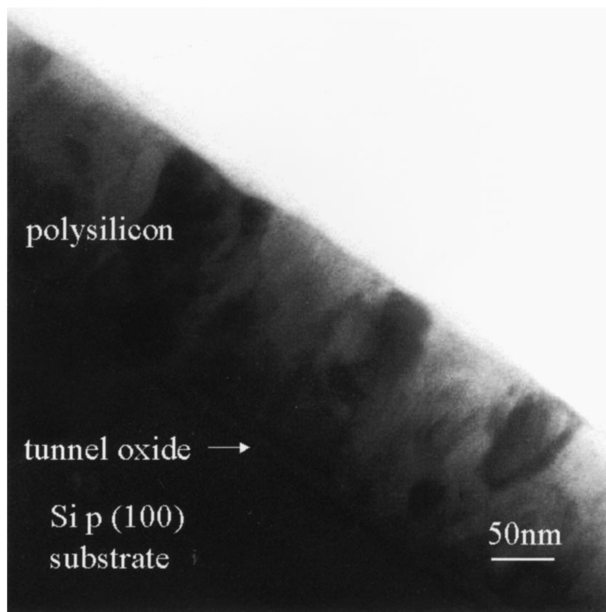

Figure 4 Low magnification bright-field XTEM picture of a N_2^+ implanted test specimen with 110 Å tunnel oxide and 1500 Å polisilicon on a Si p (100) subtrate. Smaller grains were seen at the film surface as a result of nucleation.

carbon in the bulk P^+-Si due to diffusion is therefore less than that of phosphorus. Though diffused species could contribute to grain boundary pinning; the multiplicity of small grains near the film surface demonstrates that nucleation during the high-temperature anneal dominates the microstructure and grain growth. The surface of the film is in consequence comparatively smooth with smaller grains at the surface. This is confirmed by AFM RMS results of the specimens after high-temperature treatment.

The experimental results demonstrate the effectiveness of the surface implant in nucleation and surface smoothing. Further work is needed to optimize the con-

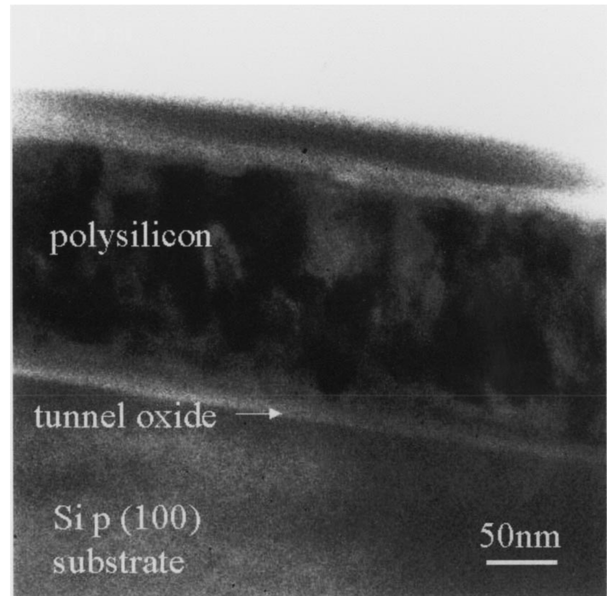

Figure 5 Low magnification bright-field XTEM picture of an Ar^+ implanted test specimen with 110 Å tunnel oxide and 1500 Å polysilicon on a Si p (100) substrate. Small surface grains were also seen as a result of nucleation.

centrations of Si_xN_y and SiC for smoothing. Here only saturated N_2^+ and Ar^+ doses of 1×10^{16} cm^2 were studied. The concentrations of the Si_xN_y or SiC should be adequate to generate an optimum number of nucleating centers at the surface and yet not to self-coagulate during annealing. By changing the energy of the ion implantation, one can vary the concentrations of the implanted species.

In conclusion, a technique to improve the smoothness of the floating polysilicon layer of non-volatile memory devices has been proposed. Via low-energy N_2^+ and Ar^+ ion implantation onto exposed deposited-polysilicon film, Si_xN_y and SiC are formed at the top surface of the film. These silicon impurities act as additional nucleating centers in the film, promoting growth of small surface grains in the event of a following high-temperature process step. Better planarity of the film is achieved and this implies the generation of a good interface with the subsequently deposited or thermally grown interpoly dielectric. The results are promising for the control of surface roughness by Low-Energy Ion Implantation.

Acknowledgments

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