High Spatial Resolution Strain Measurement of Deep Sub-micron Semiconductor Devices Using CBED

Suey Li Toh[1,2,3], K. Li[1], C.H. Ang[1], E. Er[1], S. Redkar[1], K.P. Loh[2], C.B. Boothroyd[3] and L. Chan[1]
[1]Chartered Semiconductor Manufacturing Ltd, 60 Woodlands Ind. Park D, Street 2, Singapore 738406
[2]Department of Chemistry, National University of Singapore, 3 Science Drive 3, Singapore 117543
[3]Institute of Materials Research and Engineering, 3 Research Link, Singapore 117602
Phone: (65) 63604617 Fax: (65) 63602935 Email: likun@charteredsemi.com

Abstract – Mechanical stress due to trench isolation and contact etch-stop-layers (ESLs) has been reported to show a marked influence on the electron and hole mobility of nanoscaled MOSFETs. Conventional tools such as micro-Raman spectroscopy and X-ray diffraction for measuring strain are limited in resolution. By using convergent beam electron diffraction (CBED) with nanometer spatial resolution, we have evaluated the mechanical stress induced in deep sub-micron devices by different etch-stop-layers (ESLs) and have demonstrated that the stress along the channel region can be engineered through the implementation of different ESLs.

1. Introduction

With the scaling down of complementary metal-oxide-semiconductor (CMOS) devices, the influence of mechanical stress on the performance of deep sub-micrometer MOS field-effect transistors (MOSFETs) becomes more sensitive. Features surrounding the MOSFET channel such as shallow trench isolation (STI) [1], sidewall spacer and ESLs [2] generate considerable amounts of distortion in the underlying silicon. New approaches such as the use of a strained poly silicon gate electrode [3] or using Ge implantation to reduce the compressive etch-stop nitride stress [4] have been proposed to tackle the problems of mechanical stress. However, most of the studies are based on simulations and electrical characterization and very few direct measurements are carried out. Nevertheless, to understand the influence of various stages of integrated circuit processing on the device performance, quantification of the strain with nanometer-scale accuracy is necessary. Typical methods for analyzing strain such as micro-Raman spectroscopy and X-ray diffraction have spatial resolution in the micrometer range, hence are unsuitable for characterizing nanoscaled devices.

In this paper, we use CBED with a probe size as small as a few nanometres to detect the local lattice strain for deep sub-micrometer technologies. The CBED pattern comprises higher-order Laue zone (HOLZ) lines, which are very sensitive to changes in lattice parameter and thus is a powerful tool for obtaining the local lattice strain. For our study, this technique was applied to the quantification of the strain induced by various ESLs along the channel region. Besides this, we also give detailed descriptions of the experimental procedures that are necessary to obtain distinct HOLZ line patterns which will facilitate the simulation of the diffraction patterns to obtain the strain components.

2. Experimental

In this work, a comparison was made between two contact ESL films: (a) a single layer of 300 Å Si_3N_4, and (b) a stacked layer comprising of 200 Å silicon oxynitride (SiO_xN_y) capped with 300 Å Si_3N_4. The devices analyzed were n-channel MOSFETs with channel width/length (W/L) of 10/0.12 µm, fabricated using 0.13µm CMOS technology. The Si_3N_4 and SiO_xN_y were deposited by plasma-enhanced chemical vapour deposition (PECVD) at 480-550 ^oC, using SiH_4/N_2 and $SiH_4/N_2/N_2O$ gases, respectively.

The specimens were first prepared by manually polishing the sample to a thickness of 30 µm in the [110] direction. After polishing, the pre-thinned sample was glued onto a copper grid and focused ion beam (FIB) milling was applied until the area of interest was about 0.25 µm thick. A schematic diagram for the specimen resulting from the above preparation steps is shown in Fig. 1. This method allows the direct electron beam through the specimen and hence aids considerably in improving the contrast of the HOLZ lines obtained. In addition, the thickness of the sample can be monitored. Uniformity of the thickness is very critical for ensuring reliable CBED strain measurements. Furthermore, this procedure also allows the use of plasma cleaning of the specimens before loading into the transmission electron microscope (TEM). This helps to further enhance the clarity of the patterns.

A Tecnai F20 TEM equipped with a field-emission gun (FEG) and a Gatan imaging filter (GIF), was used to capture the CBED patterns. The scanning transmission electron microscopy (STEM) mode was used to collect CBED patterns at specific locations with a probe size of about 2 nm. The use of energy filtering for zero-energy-loss imaging reduces the background inelastic scattering considerably so that the contrast in the CBED patterns is enhanced when taken at room temperature. An operating voltage of 200 kV and a <230> zone axis were used. The <230> beam direction was chosen as it requires a tilt angle of only 11.3° from the <110> orientation and the projection effect induced along the direction normal to the wafer axis is much smaller than that for the alternative <130> zone axis. This is especially critical when the device dimensions continue to be scaled down.

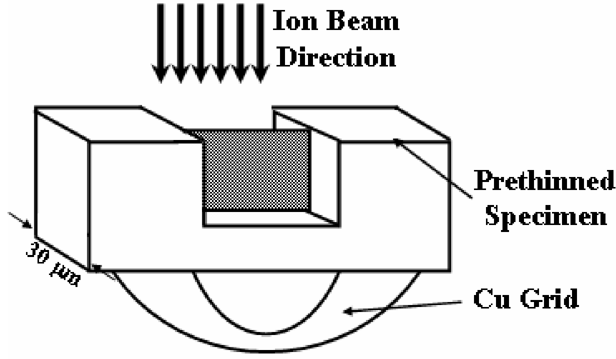

Fig. 1. A sketch of the pre-thinned specimen during further thinning using focused ion beam milling.

2. Procedures for Strain Analysis

Strain distributions were extracted from the CBED patterns using the JEMS software package of Stadelmann [5]. Using a Si CBED pattern taken from the substrate, the effective acceleration voltage and camera length were determined. Subsequently, CBED patterns were taken from the region to be analyzed. The lattice parameters were determined by comparison with simulations and used for calculation of the strain components.

The strain tensor components can be calculated from the crystal lattice parameters ($a_X, a_Y, a_Z, \alpha, \beta$ and γ) as follows:

$$\varepsilon_{ii} = \frac{a_i - a_{Si}}{a_{Si}} \qquad \text{with } i = \text{X, Y, Z}$$

$$\varepsilon_{XY} = \frac{\frac{\pi}{2} - \gamma}{2}, \varepsilon_{XZ} = \frac{\frac{\pi}{2} - \beta}{2}, \varepsilon_{YZ} = \frac{\frac{\pi}{2} - \alpha}{2} \tag{1}$$

with a_0 = 0.5431 nm, the lattice parameter of perfect silicon.

Since the structures are grown on the silicon wafers along the <110> direction, the same amount of distortion will be induced along the [100] and [010] crystallographic directions and the following relation is obtained:

$$a_X = a_Y \tag{2}$$

Incorporation of the contact etch-stop silicon nitride layer exerts a uniaxial strain channel [2], therefore the planar strain approximation, where the deformations are assumed to take place in the x-z plane (see Fig. 2), can be assumed and the following conditions can be derived:

$$\alpha = 180° - \beta \tag{3}$$

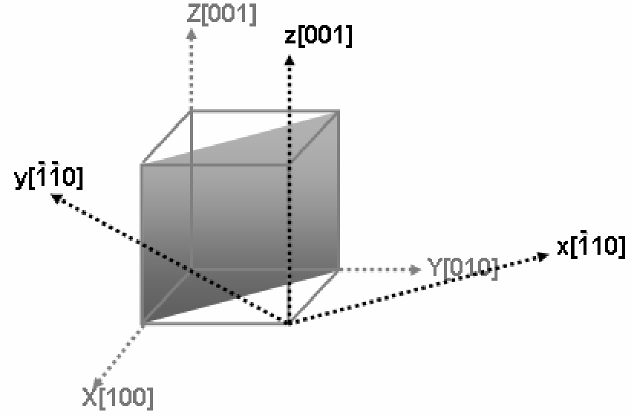

Fig. 2. A schematic representation of the orientation of the device. Two crystallographic systems are shown: (i) crystal axes (X$[100]$, Y$[010]$ and Z$[001]$), and (ii) real structure axes (x$[\bar{1}10]$, y$[\bar{1}\bar{1}0]$ and z$[001]$). The beam is along y$[\bar{1}\bar{1}0]$.

$$\frac{\Delta a_X}{a_X} = \frac{\Delta a_Y}{a_Y} = -\frac{\Delta\gamma}{2} \tag{4}$$

Using the above conditions, the number of unknowns can be reduced from 6 to 3. When the coordinates are transformed from the original crystallographic plane (X$[100]$, Y$[010]$ and Z$[001]$) about the Z-axis to those in a real device structure, the expressions for the horizontal (ε_x) and vertical (ε_y) strain tensors will be as shown in (5) and (6) below, where the angle θ is defined to be the deviation from the X$[100]$ axis:

$$\varepsilon_x = \frac{\varepsilon_{XX} + \varepsilon_{YY}}{2} + \frac{\varepsilon_{XX} - \varepsilon_{YY}}{2}\cos 2\theta + \frac{\gamma_{XY}}{2}\sin 2\theta \tag{5}$$

$$\varepsilon_y = \frac{\varepsilon_{XX} + \varepsilon_{YY}}{2} - \frac{\varepsilon_{XX} - \varepsilon_{YY}}{2}\cos 2\theta - \frac{\gamma_{XY}}{2}\sin 2\theta \tag{6}$$

As shown in Fig. 2, for the real structure, the axes system is defined as x$[\bar{1}10]$, y$[\bar{1}\bar{1}0]$ and z$[001]$. The x and y axes are rotated by 135° about the Z axis from the XY axes position. By substituting θ = 135° and θ = 225° into (5) and (6) respectively, we obtain:

$$\varepsilon_x = \frac{1}{2}\varepsilon_{XX} + \frac{1}{2}\varepsilon_{YY} - \varepsilon_{XY} \tag{7}$$

$$\varepsilon_y = \frac{1}{2}\varepsilon_{XX} + \frac{1}{2}\varepsilon_{YY} + \varepsilon_{XY} \tag{8}$$

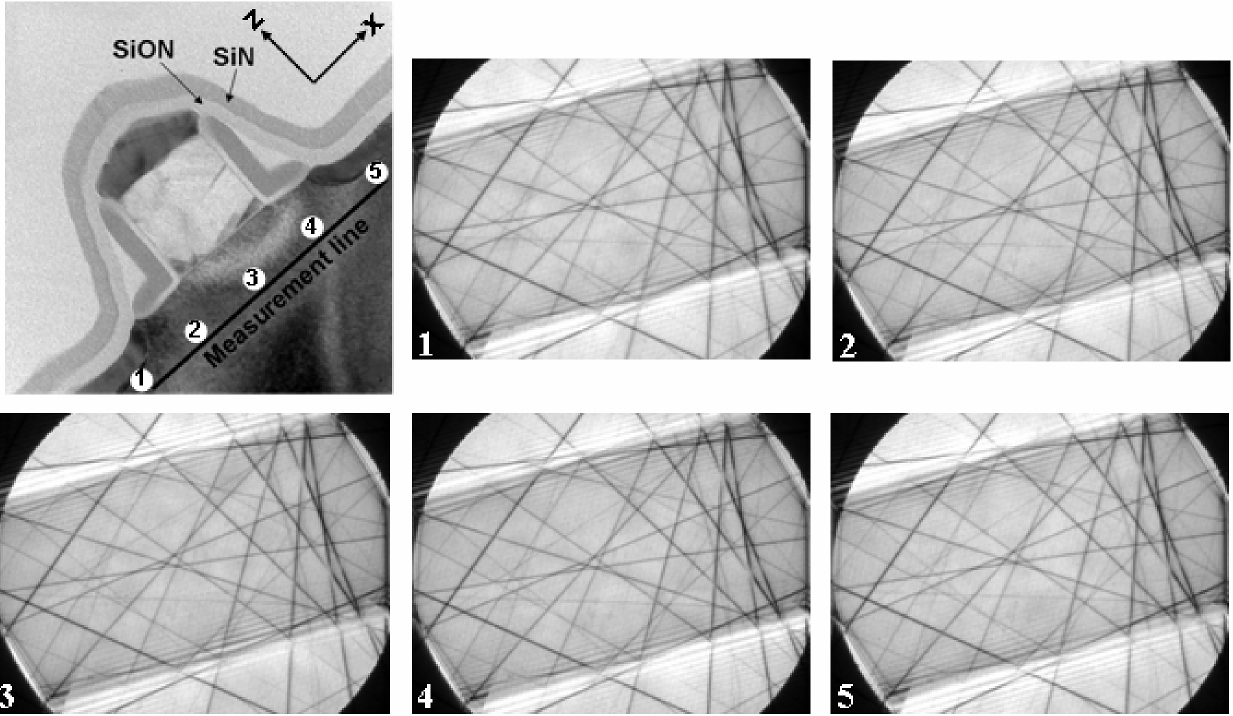

Fig. 3. Cross-sectional bright-field TEM image of an n-channel MOSFET with Si_3N_4/ SiO_xN_y ESL films. The CBED patterns, numbered from 1 to 5, are taken at the <230> zone axis from the measurement line marked on the bright-field image.

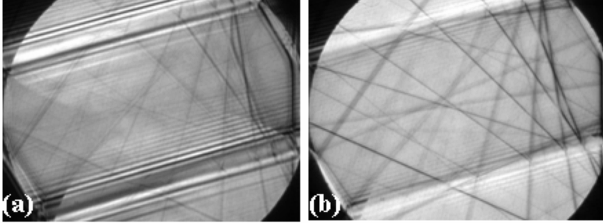

Fig. 4. Examples of CBED patterns obtained with the probe near an interface with a steep stress gradient showing (a) blurred and (b) split HOLZ lines.

$$\varepsilon_z = \varepsilon_Z \tag{9}$$

ε_y is zero because of the constraint imposed by the planar strain approximation. A positive sign of the strain component is associated with a tensile strain and a negative sign with a compressive strain.

3. Results and discussion

Fig. 3 shows a cross-sectional TEM image of a MOSFET with a stacked nitride ESL film. The x-axis is taken to be along the channel, while the z-axis is normal to the substrate surface. Altogether, five positions from the source to the drain contacts are examined from the measurement line indicated and the CBED patterns (numbered 1 to 5) obtained are as shown in Fig. 3. When the beam was placed too close to the interface, the large distortions in the silicon substrate meant that distinct HOLZ lines could not be obtained. Fig. 4 shows some examples of CBED patterns from such highly strained regions.

Fig. 5a shows a comparison of the ε_x strain variation from the Si_3N_4/ SiO_xN_y and Si_3N_4 ESL samples. For positions below the source and drain contacts (positions 1 and 5), the lattice strain is tensile (ε_x >0) as a compressive overlayer typically yields a tensile strain in the substrate underneath. However, directly under the gate electrode (position 3), a compressive strain is obtained (ε_x <0). This has been attributed to the geometric effect whereby the lattice strain under the gate electrode for a short-channel transistor was determined predominantly by the stress from the sidewall of the gate electrode exerted from the ESL [6]. From the results, we can see that the Si_3N_4 ESL sample exhibited a larger spatial variation of the ε_x strain when compared to the Si_3N_4/ SiO_xN_y ESL sample. This suggests that by incorporating a thin SiO_xN_y buffer film beneath the Si_3N_4 ESL, the stress induced by the Si_3N_4 film along the transistor channel is relieved to a certain extent. The corresponding ε_y strain distributions for the Si_3N_4/ SiO_xN_y and Si_3N_4 ESL samples are depicted in Fig. 5b. Comparing with Fig. 5a, it can be observed that the magnitude of ε_y is opposite to that of ε_x as strain in one direction would

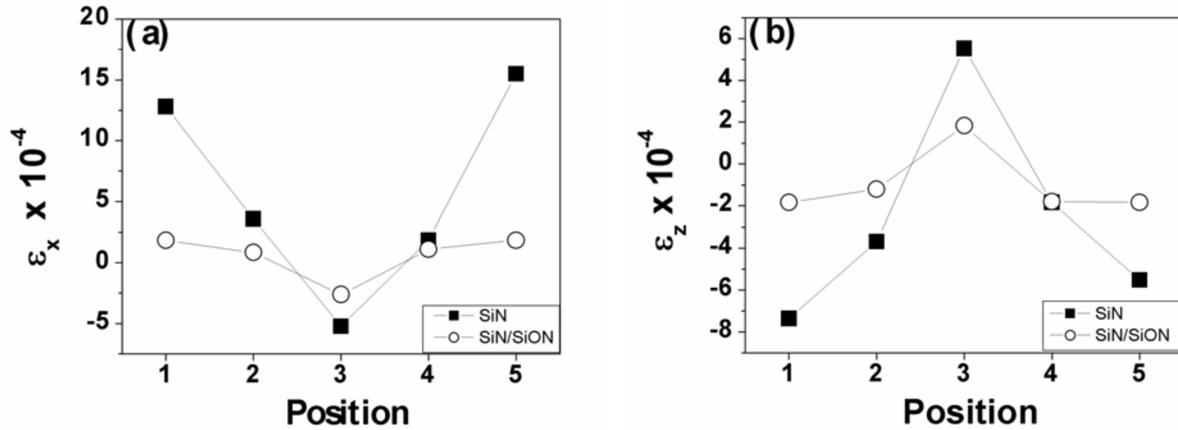

Fig. 5. (a) Lateral lattice strain ε_x , and (b) transverse lattice strain ε_y , obtained after simulation using JEMS software for Si_3N_4/ SiO_xN_y and Si_3N_4 ESL samples measured from the CBED patterns taken from the Si substrate at the positions indicated by the numbers from 1 to 5 in Fig. 2.

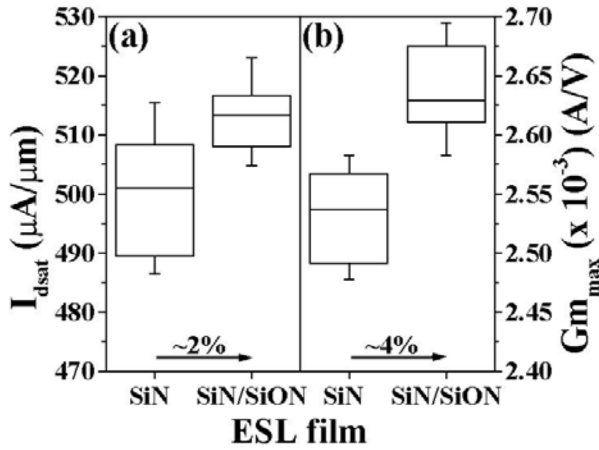

Fig. 6. Comparison of (a) saturation drain current (I_{dsat}) and (b) maximum transconductance (Gm_{max}) between Si_3N_4/ SiO_xN_y and Si_3N_4 ESL samples for n-channel MOSFETs in the form of a box plot.

result in an opposite trend in the perpendicular direction.

The effect of the relief of the compressive strain in the transistor channel on the electrical conduction of the n-channel MOSFET is shown in Fig. 6 in the form of a box plot, whereby a comparison of the saturation drain current (I_{dsat}) and maximum transconductance (Gm_{max}) was made between the Si_3N_4/ SiO_xN_y and Si_3N_4 ESL samples. As seen from Fig. 6 the Si_3N_4/ SiO_xN_y ESL sample had a higher I_{dsat} (~2 %) and Gm_{max} (~4 %) than the Si_3N_4 ESL sample. This is a consequence of reducing the compressive strain in the transistor channel region by the buffering effect offered by the SiO_xN_y layer.

4. Conclusion

In summary, we have demonstrated that CBED is capable of performing high spatial resolution strain measurement along the channel region in deep sub-micron MOSFETs and the results show that the stress at the channel region could be engineered through the implementation of different ESLs. By introducing a thin buffer layer of SiO_xN_y underneath the Si_3N_4 contact ESL, the compressive channel strain in the deep sub-micron MOSFET could be relieved. This reduction in the channel stress has resulted in an improvement in the electrical performance of n-channel MOSFETs.

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