Electrochemical and Solid-State Letters, **8** (2) G38-G40 (2005)
1099-0062/2004/8(2)/G38/3/$7.00 © The Electrochemical Society, Inc.

Reduction of Local Mechanical Stress in a Transistor Using Si_3N_4/SiO_xN_y Contact ESL

Suey Li Toh,[a,z] K. P. Loh,[a] C. B. Boothroyd,[b] K. Li,[c] C. H. Ang,[c] E. Er,[c] and L. Chan[c]

[a]*Department of Chemistry, National University of Singapore, Singapore 117543, Singapore*
[b]*Institute of Materials Research and Engineering, Singapore 117602, Singapore*
[c]*Chartered Semiconductor Manufacturing Limited, Singapore 738406, Singapore*

We have investigated the influence of a contact etch-stop layer (ESL) on the local mechanical stress in a deep sub-micrometer complementary metal oxide semiconductor (CMOS) field-effect transistor using convergent-beam electron diffraction with nano-scale resolution. By introducing a thin buffer layer of SiO_xN_y underneath the Si_3N_4 contact ESL, we have shown that the compressive channel strain can be effectively mitigated, resulting in higher electron mobility and drive current in n-channel metal oxide semiconductor field-effect transistors, without undue impact on the electrical performance of p-channel transistors. Hence, the Si_3N_4/SiO_xN_y film stack is a promising alternative for contact ESL to enable high-performance CMOS devices.
 [DOI: 10.1149/1.1843754]

Manuscript submitted July 5, 2004; revised manuscript received August 4, 2004. Available electronically December 14, 2004.

The borderless contact process utilizing a contact etch-stop layer (ESL) has been widely employed in advanced complementary metal oxide semiconductor (CMOS) technology to minimize chip size as design rules scale down.[1,2] However, it has been reported in recent years that the performance of deep sub-micrometer MOS field-effect transistors (MOSFETs) is markedly influenced by the mechanical stress generated from the contact ESL in the channel region.[3-6] Specifically, conventional plasma-enhanced chemical vapor deposited (PECVD) Si_3N_4 ESL generally induces considerable compressive stress in miniaturized MOSFETs, resulting in electron mobility degradation.[5,6] To overcome the deleterious effect of the Si_3N_4 ESL, several solutions have been proposed in the past. Ito *et al.* claimed that n-channel MOSFET performance could be improved by altering the PECVD Si_3N_4 film stress from compressive to tensile, however at the expense of p-channel MOSFET performance.[5] On the other hand, Shimizu *et al.* reported that Si_3N_4 ESL induced compressive stress in n-channel MOSFETs could be largely relaxed using selective Ge implantation into the Si_3N_4 layer.[6] In this paper, we report a simple local mechanical stress reduction approach by incorporating a thin buffer layer of PECVD silicon oxynitride (SiO_xN_y) underneath the compressive Si_3N_4 ESL film. The proposed SiN/SiO_xN_y ESL improves the performance of n-channel MOSFETs without affecting the p-channel MOSFET performance. The local mechanical stress reduction in the transistor channel is verified using convergent-beam electron diffraction (CBED) with nano-scale resolution.[7,8] Additionally, we show that the lattice strain variation along the channel is significantly reduced using the Si_3N_4/SiO_xN_y ESL film.

Experimental

The devices were n- and p-channel MOSFETs with channel width/length (W/L) of 10/0.12 μm, fabricated using 0.13 μm CMOS technology. To demonstrate the local mechanical stress reduction in the transistor channel using Si_3N_4/SiO_xN_y ESL, two contact ESL films were evaluated in this study: (A) a single 300 Å layer of Si_3N_4, and (B) a stacked layer comprising of 200 Å silicon oxynitride (SiO_xN_y) capped with 300 Å Si_3N_4. The Si_3N_4 and SiO_xN_y were deposited by PECVD at 480-550°C, using SiH_4/N_2 and $SiH_4/N_2/N_2O$ gases, respectively. An *in situ* process recipe has been developed for forming the Si_3N_4/SiO_xN_y film. CBED patterns were captured using a Tecnai F20 transmission electron microscope (TEM) equipped with a field-emission gun (FEG) and a Gatan imaging filter (GIF). Scanning transmission electron microscopy (STEM) mode was used to collect CBED patterns at specific locations with a probe size of about 2 nm. The use of energy filtering to collect zero-energy-loss images reduces the background inelastic scattering considerably so that the contrast in the CBED patterns is enhanced when taken at room temperature. A cross-sectional TEM image of a MOSFET with the CBED measurement positions indicated is depicted in Fig. 1a. A typical CBED pattern obtained from one of these locations is illustrated in Fig. 1b. Distinct higher-order Laue zone (HOLZ) lines could be readily observed on the CBED pattern, facilitating the extraction of lattice strain components, εxx and εyy, using the EMS software package.[9] The typical standard deviation of the measured strain was 1.8×10^{-4}.[8] In determining εxx and εyy the x-axis is taken along the channel, and the y-axis is normal to the substrate surface. A positive sign of the strain component is associated with a tensile strain, while a negative sign indicates a compressive strain.

Results and Discussion

Figure 2a compares the εxx strain variation measured from the source to the drain contacts, between the Si_3N_4/SiO_xN_y and the Si_3N_4 ESL samples. The Si_3N_4 ESL sample exhibited a large spatial variation of the εxx strain. Below the source and drain contacts (locations 1 and 5), the lattice strain showed a relatively high tensile stress ($\varepsilon xx > 0$). This has been attributed to the fact that a compressive overlayer generally yields a tensile strain in the substrate underneath.[10] In contrast, directly under the gate electrode (location 3), the lattice strain has changed from tensile to compressive ($\varepsilon xx < 0$). Our observation is in agreement with a previous study asserting that the lattice strain under a gate electrode of a short-channel transistor was predominately dictated by the stress from the sidewall of the gate electrode exerted from the ESL.[5] On the other hand, the lateral strain profile of the Si_3N_4/SiO_xN_y ESL sample displayed significantly smaller variation when compared to that of the Si_3N_4 ESL sample, as seen in Fig. 2a. Furthermore, the locations below the source/drain contacts and gate electrode have much smaller strain magnitudes than for the Si_3N_4 ESL sample. Hence, the incorporation of a SiO_xN_y film beneath a Si_3N_4 ESL aids considerably in cushioning the compressive stress induced by the Si_3N_4 film in the transistor channel. The result is consistent with the blanket film stress measurements for different wafers with varying nitride thickness listed in Fig. 2a. The blanket film stresses measured using the wafer bowing technique were approximately −80 and −40 MPa for the 300 Å Si_3N_4 and the 300 Å Si_3N_4/200 Å SiO_xN_y layers, respectively. Thus, the Si_3N_4 film produced a higher compressive stress than the Si_3N_4/SiO_xN_y stacked film, in agreement with the CBED result shown in Fig. 2a. The compressive stress relief in the transistor channel is expected to influence the electrical conduction of the MOSFET, as shown later. Figure 2b depicts the

[z] E-mail: g0202196@nus.edu.sg

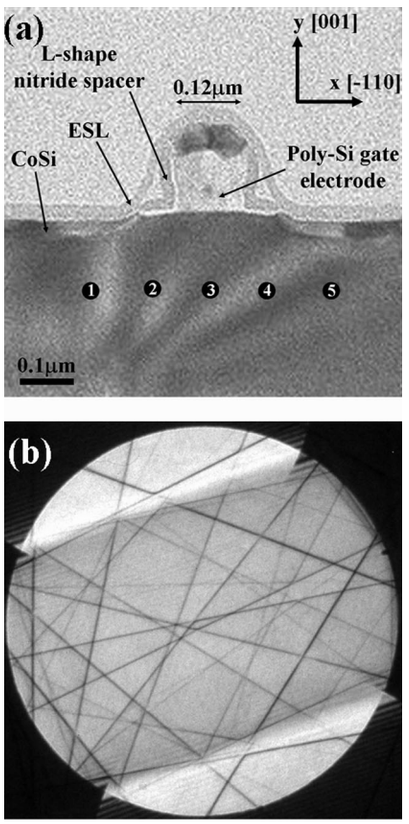

Figure 1. (a) Cross-sectional bright-field TEM image of an n-channel MOSFET with the CBED measurement positions indicated by the numbers 1 to 5. (b) An example of one of the CBED patterns obtained from the sample shown in (a) with the electron beam aligned along the ⟨230⟩ zone axis.

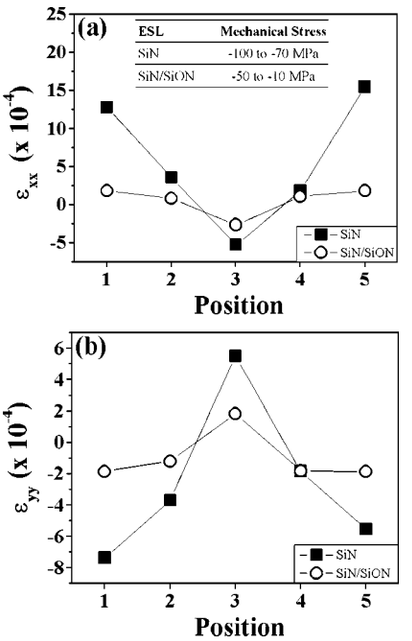

Figure 2. (a) Longitudinal lattice strain εxx, and (b) transverse lattice strain εyy for Si_3N_4 and Si_3N_4/SiO_xN_y ESL samples measured from CBED patterns taken from the Si substrate at the positions indicated by the numbers 1 to 5 on Fig 1a. Inset in (a) shows the blanket film stress measurement for Si_3N_4 and Si_3N_4/SiO_xN_y films.

corresponding εyy strain distribution for the Si_3N_4 and the Si_3N_4/SiO_xN_y ESL samples. Comparing with Fig. 2a, it is evident that the magnitude of εyy is opposite to that of εxx. This is attributed to the fact that compressive strain in one direction typically results in a tensile strain in the perpendicular direction.

Figure 3 shows a comparison of the n-channel MOSFET saturation drain current (I_{dsat}) and maximum transconductance (Gm_{max}) between the Si_3N_4/SiO_xN_y (Fig. 3a) and Si_3N_4 (Fig. 3b) ESL samples. The (I_{dsat}) was measured at the bias condition $V_{ds} = V_{gs} = 1.2$ V while grounding the source and substrate terminals. The (Gm_{max}) was extracted from the I_d-V_g characteristics measured with $V_{ds} = 0.05$ V. Because $Gm_{max} \approx (W/L)\mu C_{ox}V_{ds}$, it tracks the effective carrier mobility (μ) in the transistor channel because the transistor size and gate capacitance (C_{ox}) were identical for both the Si_3N_4/SiO_xN_y and the Si_3N_4 ESL samples. The electrical measurements were performed on many die across a wafer. As seen from Fig. 3a and b, it is clear that the Si_3N_4/SiO_xN_y ESL sample had a higher (I_{dsat}) (~2%) and (Gm_{max}) (~4%) than the Si_3N_4 ESL sample. This observation is attributed to the Si_3N_4/SiO_xN_y ESL sample having a higher electron mobility than the Si_3N_4 ESL sample, as a consequence of reduced compressive strain in the transistor channel region due to the SiO_xN_y buffering effect shown in Fig. 2a. Note that this is the first direct experimental evidence that the local channel strain in a deep sub-micrometer n-channel MOSFET is influenced by the ESL stress, and that the stress in turn affects the electrical conduction of the transistor. Additionally, it can be inferred from Fig. 2a and 3 that the lattice strain below the source/drain contacts has minimal impact on the electrical performance of a MOSFET, as Si_3N_4 ESL has a significantly higher tensile strain below the source/drain contacts without a corresponding improvement in electrical performance. In Fig. 4 the p-channel MOSFET electrical performance of Si_3N_4/SiO_xN_y and Si_3N_4 ESL samples are compared. It can be seen that the introduction of the SiO_xN_y layer has no discernible influence on the electrical performance of the p-channel MOSFETs. This may be attributed to the piezoresistive effect, in which the stress components along the channel length and channel width act adversely against each other to determine the performance of p-channel MOSFET and this may result in minimal effect on the hole mobility.[3,11,12] The stress exerted by the nitride capping layer may not be completely uniaxial which we normally presume. In reality, it is usually a combination of both uniaxial and biaxial stresses.

The stress relief effect of SiO_xN_y film can be explained by the more relaxed structural configuration of the non-stoichiometric SiO_xN_y film. The structural configuration of a Si_3N_4 film consists of a Si-N_4 network, while a SiO_xN_y film comprises a combination of

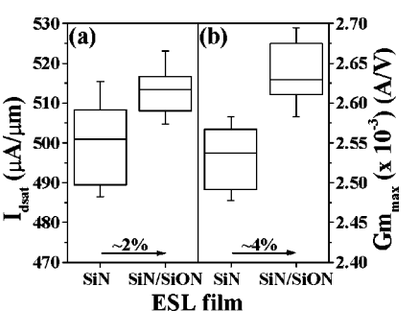

Figure 3. Comparison of (a) saturation drain current (I_{dsat}) and (b) maximum transconductance (Gm_{max}) between Si_3N_4 and Si_3N_4/SiO_xN_y ESL samples, for n-channel MOSFETs, in the form of a box plot. The plot allows the exploration of the maximum, upper quartile, median, lower quartile, and minimum values in the data set. The Si_3N_4/SiO_xN_y ESL sample depicts an improvement of ~2% and ~4% in the (I_{dsat}) and (Gm_{max}), respectively.

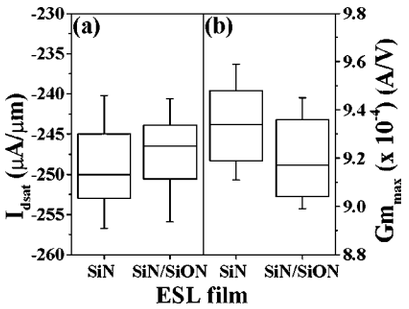

Figure 4. Comparison of (a) saturation drain current (I_{dsat}) and (b) maximum transconductance (Gm_{max}) between Si_3N_4 and Si_3N_4/SiO_xN_y ESL samples, for p-channel MOSFETs, in the form of a box plot. The ESL shows no appreciable effect on the electrical behavior.

N-Si-O_3, N_2-Si-O and N_3-Si-O networks. As a result, a Si_3N_4 film is rendered more rigid by the necessity of nitrogen forming three, rather than two, bonds as in the case of a SiO_xN_y film. The presence of the oxygen atom adds flexibility to the nitride lattice, resulting in a more relaxed structure. This may aid in the relief of the compressive stress in the Si_3N_4 film.

Conclusion

In summary, we have demonstrated, using CBED, that the compressive channel strain in a deep-sub micrometer MOSFET could be relieved by introducing a thin buffer layer of SiO_xN_y underneath the Si_3N_4 contact ESL. We have further shown that the channel stress reduction has benefited the electron mobility and drive current in n-channel MOSFETs, but without significant impact on the electrical performance of p-channel transistors. Hence, an optimized Si_3N_4/SiO_xN_y contact ESL process could offer a simple promising alternative to permit high device performance in deep sub-micron CMOS technology. Moreover, the etch selectivity required for ESL would not be unduly compromised since the SiO_xN_y layer is capped with a robust etch-stop Si_3N_4 layer.

Acknowledgments

The authors thank Dr. P. S. Lee for the wafers, L. Goh for providing the blanket film stress measurement data, C. Kon for his assistance in the sample preparation, and K. C. Tee and S. K. Wang for valuable discussions.

Chartered Semiconductor Manufacturing assisted in meeting the publication costs of this article.

References

1. B. Descouts, in *Proceedings of the VMIC Conference*, IEEE, p. 640 (1998).
2. W. C. Liu, K. B. Thei, W. C. Wang, H. J. Pan, S. G. Wuu, M. T. Lei, C. S. Wang, and S. Y. Cheng, *IEEE Electron Device Lett.*, **21**, 344 (2000).
3. F. Ootsuka, S. Wakahara, K. Ichinose, A. Honzawa, S. Wada, H. Sato, T. Ando, H. Ohta, K. Watanabe, and T. Onai, *Tech. Dig. - Int. Electron Devices Meet.*, **2000**, 575.
4. K. Goto, Y. Tagawa, H. Ohta, H. Morioka, S. Pidin, Y. Momiyama, K. Okabe, H. Kokura, S. Inagaki, Y. Kikuchi, M. Kase, K. Hashimoto, M. Kojima, and T. Sugii, in *Symposium on VLSI Technology*, IEEE, 49 (2003).
5. S. Ito, H. Namba, T. Hirata, K. Ando, S. Koyama, N. Ikezawa, T. Suzuki, T. Saitoh, and T. Horiuchi, *Microelectron. Reliab.*, **42**, 201 (2002).
6. A. Shimizu, K. Hachimine, N. Ohki, H. Ohta, M. Koguchi, Y. Nonaka, H. Sato, and F. Ootsuka, *Tech. Dig. - Int. Electron Devices Meet.*, **2001**, 19.4.1.
7. A. Toda, N. Ikarashi, H. Ono, S. Ito, T. Toda, and K. Imai, *Appl. Phys. Lett.*, **79**, 4243 (2001).
8. A. Toda, N. Ikarashi, and H. Ono, *J. Cryst. Growth*, **210**, 341 (2000).
9. P. A. Stadelmann, *Ultramicroscopy*, **21**, 131 (1987).
10. Y. G. Wang, D. B. Scott, J. Wu, J. L. Waller, J. Hu, K. Liu, and V. Ukrantsev, *IEEE Trans. Electron Devices*, **50**, 529 (2003).
11. C.-H. Ge, C.-C. Lin, C.-H. Ko, C.-C. Huang, Y.-C. Huang, B.-W. Chan, B.-C. Perng, C.-C. Sheu, P.-Y. Tsai, L.-G. Yao, C.-L. Wu, T.-L. Lee, C.-J. Chen, C.-T. Wang, S.-C. Lin, Y.-C. Yeo, and C. Hu, *Tech. Dig. - Int. Electron Devices Meet.*, **2003**, 3.7.1.
12. G. Scott, J. Lutze, M. Rubin, F. Nouri, and M. Manley, *Tech. Dig. - Int. Electron Devices Meet.*, **1999**, 827.