Strain analysis in silicon substrates under uniaxial and biaxial stress by convergent beam electron diffraction

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A detailed description of the application of the convergent beam electron diffraction (CBED) technique for studying strain propagation in the $Si_{1-x}Ge_x/Si$ blanket wafers as well as silicon-based metal–oxide–semiconductor field-effect transistors is presented. Specifically, a simple and robust experimental procedure and analysis for silicon lattice strain measurement using the CBED technique is detailed in this article. The use of focused ion beam milling allows for better control of the thickness and site-specific analysis, especially for nanoscaled devices. A pictorial representation of the analytical conditions for the higher order Laue zone lines in CBED patterns is also reported in this work. Based on the Si lattice strain measurement results, we determined that a thin buffer layer of SiO_xN_y incorporated below the Si_3N_4 overlay film could render the uniaxial channel strain less compressive. Stress studied on $Si_{1-x}Ge_x/Si$ blanket wafers reveals that a steeper SiGe compositional gradient would induce larger biaxial strain in the underlying Si substrate and hence a smaller amount of misfit dislocations. © *2005 American Vacuum Society.*
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I. INTRODUCTION

To have a better understanding of the interfacial stress on the underlying substrate, there is a need for strain characterization down to the nanoscale volume of the sample. Conventional stress measurement tools such as micro-Raman spectroscopy and x-ray diffraction are typically concerned with the macroscopic picture and give us an averaged value. Point-to-point quantification of the strain would therefore allow a spatially resolved measurement of stress propagation in the solid. This would provide us with a means of tailoring the amount of strain in the substrate by adjusting the processing conditions or the dimensions of the neighboring geometric structures.

Presently, a technique based on analyzing the shift in higher order Laue zone (HOLZ) lines in convergent beam electron diffraction (CBED) patterns is the only strain measurement method capable of determining localized strain fields. The positions of these lines are very sensitive to changes in lattice parameters.[1] Using this technique, Toda *et al.* analyzed the stress induced by the shallow trench isolation (STI) in nanoscaled devices and obtained a good correlation between the strain distribution in the channel region and the electrical characteristics.[2] On the other hand, Stuer *et al.* reported the influence of processing conditions on the strain distribution at different layers before the devices are processed fully, and showed that wet pregate oxidation coupled with small structures increased the stress around the STI structures.[3,4]

Despite the increasing interest and reports on CBED strain measurement, little attention was paid in the past to the experimental and the analytical procedures. There are some inherent technical problems associated with the CBED strain measurement technique which are not explicitly mentioned in the past reports. For instance, conventional sample preparation standard procedures which include sawing, gluing, ultrasonic drilling, mechanical lapping, dimpling, and ion beam milling to perforation, if used for nanoscaled devices, may not allow precise control of the location and sample geometry. Moreover, the methods may not allow good control of the thickness of the sample and are time consuming. Furthermore, the diffraction pattern quality depends on the thickness of the sample in the analyzed region. If the specimen is too thin, the HOLZ lines become broad and their contrast is reduced markedly. On the contrary, if the specimen is too thick, there is too little intensity in the CBED pattern. In addition to technical difficulties in sample preparation, the basis for the underlying assumptions used in the analysis of the CBED patterns is not clearly stated. In particular, the differences in the analytical conditions between uniaxial and biaxial strain have not been clearly elucidated.

In this article, we describe a simple and robust sample preparation procedure for CBED strain measurement. Additionally, we also provide pictorial representation of the analytical conditions for uniaxial and biaxial stress effect during

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the simulation. The uniaxial strain analysis was applied to quantify the mechanical strain induced by different overlay nitride films along the channel region in which the overlay film was assumed to exert a one-dimensional strain onto the channel.[5,6] On the other hand, the biaxial analysis was implemented on the $Si_{1-x}Ge_x/Si$ heterostructures to obtain the intrinsic strain values in which the top SiGe film exerts a biaxial stress on the underlying silicon substrate due to lattice mismatch.[7] The localized strain results obtained for the different nitride films correlate well with other characterization data like macroscopic wafer curvature stress measurement and electrical performance. The biaxial strain results obtained for $Si_{1-x}Ge_x/Si$ heterostructures allows us to look into the effect of the compositional gradient of the SiGe on the equilibrium conditions of the Si substrate.

II. EXPERIMENTAL PROCEDURES FOR CBED STRAIN MEASUREMENT

A. Sample description

The effect of the uniaxial stress was investigated on *n*-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) with channel width/length (W/L) of $10/0.12\ \mu$m, fabricated using $0.13\ \mu$m complementary MOS technology. In the study, a comparison was made between two overlay nitride films: (a) a single 300 Å layer of Si_3N_4 and (b) a stacked layer comprising of a thin layer of silicon oxynitride (SiO_xN_y) capped with 300 Å Si_3N_4 deposited by plasma-enhanced chemical vapor deposition. On the other hand, the biaxial stress analysis was carried out on the $Si_{1-x}Ge_x/Si$ heterostructures deposited by low-pressure chemical vapor deposition. The Ge composition in the graded layer increased from the buffer layer to the silicon substrate. A comparative study was made between two thicknesses of the graded layer ($G1$ and $G2$) and hence different grading gradients, in which $G1$ and $G2$ samples referred to thin and thick graded layers, respectively.

B. CBED sample preparation

The use of focused ion beam (FIB) milling for sample preparation provides greater ease of aiming at the precise sample location, hence allows for site-specific analysis and offers a more robust technique of controlling the uniformity of the sample thickness. This is necessary to ensure reliable CBED strain analysis but is difficult to control using the conventional polishing method. The specimens were first prepared by manually polishing the sample to a thickness of $30\ \mu$m in the [110] direction. After polishing, the prethinned sample was glued onto a copper grid and FIB milling was applied until the area of interest was about $0.25\ \mu$m thick.[8] The relaxed fraction for a sufficiently homogeneously strained volume of the crystal, although present, is assumed to be negligible if distinct HOLZ lines are obtained.[9] This method permits a direct electron beam through the specimen and thereby aids greatly in enhancing the contrast of the HOLZ lines obtained. A copper grid that contains carbon film as is often used to contain FIB-cut transmission electron microscope (TEM) specimens, however, would reduce the resolution of the CBED patterns obtained. Additionally, the above procedure also allows the use of plasma cleaning of the specimens before loading into the microscope. This helps to clean the specimen's surface effectively and further enhance the clarity of the patterns.

C. CBED measurements

The diffraction patterns were captured using a Tecnai F20 TEM equipped with a field-emission gun and a Gatan imaging filter at an electron acceleration voltage of 200 kV in the $\langle 230\rangle$ zone axis. The scanning transmission electron microscopy mode was used to collect the CBED patterns at specific locations with a probe beam size of about 2 nm. The semiconvergence angle of the beam was about 18 mrad and the spatial resolution was estimated to be about 10 nm. Using CBED, the standard deviation of the measured strain was 1.8×10^{-4}.[1] The strain is measured by finding the best fit (minimizing χ^2 value) between the HOLZ line intersections in the experimental and the simulated diffraction patterns using the kinematical approach.[10,11] Typically, a measurement line was drawn across the region to be analyzed and the number of points to be investigated along the line was defined. An automation mode could then be set to capture the patterns and this helped to ease the process of CBED pattern acquisition. The use of energy filtering for zero-energy-loss imaging helped to reduce the background inelastic scattering considerably so that the contrast in the CBED patterns was enhanced when taken at room temperature. $\langle 230\rangle$ beam direction was chosen as it requires a tilt angle of only 11.3° from the $\langle 110\rangle$ orientation and the projection effect induced along the direction normal to the wafer axis is much smaller than that for the alternative $\langle 130\rangle$ zone axis.[9] However, the above analysis is only carried out in regions where distinct HOLZ line patterns are captured and the deformation may be relatively weak. To determine the initial stress state of the bulk structure, the stress relaxation at the surface of a specimen especially near the interfacial region, cannot be neglected.[12]

D. Strain tensor determination

For TEM analysis, θ is very small and the Bragg's diffraction law can be approximated as

$$2d_{hkl}\theta \approx \lambda, \tag{1}$$

where d_{hkl} is the interplanar spacing for the $\{hkl\}$ set of planes and θ is the Bragg angle. Since $d_{hkl}=a/\sqrt{h^2+k^2+l^2}$ for silicon which has a cubic structure and $\lambda \propto E^{-1/2}$, the following relation can be obtained:

$$a\theta \propto E^{-1/2}, \tag{2}$$

where a is the lattice constant of silicon and E is the electron acceleration voltage.

Differentiating Eq. (2) with respect to a and θ but keeping the electron acceleration voltage constant, we get

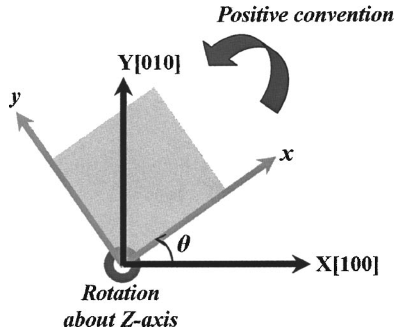

FIG. 1. Sign convention for the strains.

$$\frac{\Delta\theta}{\theta} = -\frac{\Delta a}{a}. \tag{3}$$

Differentiating Eq. (2) with respect to θ and E but keeping the lattice parameter constant (unstrained), we get

$$\frac{\Delta\theta}{\theta} = -\frac{\Delta E}{2E}. \tag{4}$$

From Eqs. (3) and (4), we can see that both lattice strain and variation in the electron acceleration voltage can induce changes in the position of the HOLZ lines. A small shift in the electron acceleration voltage can thus be misinterpreted as strain. To correct for this, it is essential to determine the effective acceleration voltage initially. This is done by simulating the CBED pattern taken from the unstrained part of the silicon substrate using the JEMS software package of Stadelmann.[13] The lattice parameters of the region to be analyzed were determined by comparison with simulations and were then used to calculate the strain components. The strain tensor components can be calculated from the crystal lattice parameters (a_X, a_Y, a_Z, α, β, and γ) as follows:

$$\epsilon_{ii} = \frac{a_i - a_{\text{Si}}}{a_{\text{Si}}}$$

with $i = X, Y, Z$

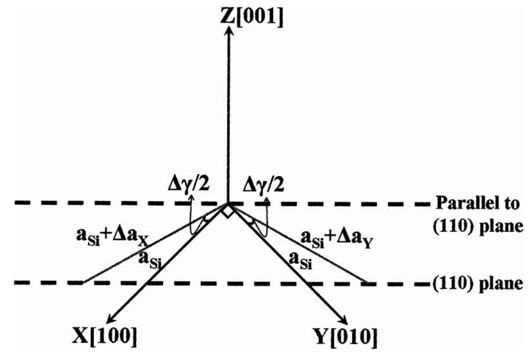

FIG. 3. Schematic representation of the device in which there is strain along the (110) plane. The relation: $\Delta a_X/a_X = \Delta a_Y/a_Y = -(\Delta\gamma/2)$ can be derived.

$$\epsilon_{XY} = \frac{\frac{\pi}{2} - \gamma}{2}, \quad \epsilon_{XZ} = \frac{\frac{\pi}{2} - \beta}{2}, \quad \epsilon_{YZ} = \frac{\frac{\pi}{2} - \alpha}{2}, \tag{5}$$

with $a_{\text{Si}} = 0.54309$ nm, the lattice parameter of perfect silicon.

Since the majority of MOSFETs are fabricated on Si (001) substrates along the $\langle 110 \rangle$ direction, the strain tensor values obtained from Eq. (5) are subsequently transformed from the original crystallographic axes ($X[100]$, $Y[010]$, and $Z[001]$) about the Z axis to those in a device axis to allow for better understanding of the influence of different material layers on the electrical performance of the devices so that a direct correlation between the strain tensors and the electrical characteristics can be established. A pictorial representation for the analytical conditions will be illustrated in Figs. 1–4. The expressions for the ϵ_x and ϵ_y strain tensors for the device structure in the $x-y$ plane are as shown in Eqs. (6) and (7), where the angle θ is defined as the deviation from the $X[100]$ axis (see Fig. 1):[14]

$$\epsilon_x = \frac{\epsilon_{XX} + \epsilon_{YY}}{2} + \frac{\epsilon_{XX} - \epsilon_{YY}}{2}\cos 2\theta + \epsilon_{XX}\sin 2\theta, \tag{6}$$

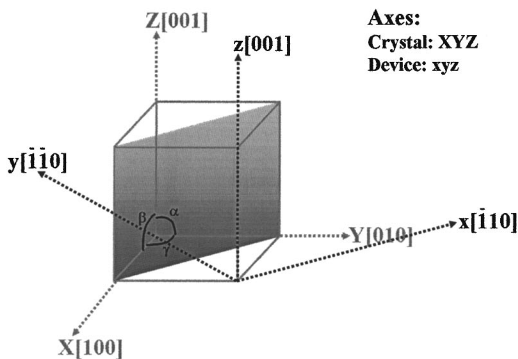

FIG. 2. Schematic representation of the orientation of the device. Two crystallographic systems are shown: (i) crystal axes ($X[100]$, $Y[010]$, and $Z[001]$), and (ii) device structure axes ($x[\bar{1}10]$, $y[\bar{1}\bar{1}0]$, and $z[001]$). The beam is along $y[\bar{1}\bar{1}0]$.

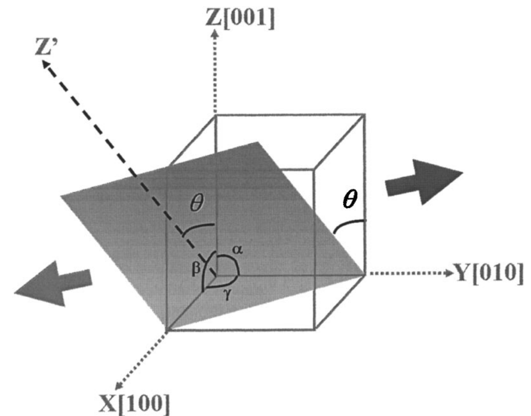

FIG. 4. Schematic representation of the device in which there is an angular distortion along the (110) plane by θ. The relation: $\alpha = 180° - \beta$ can be derived.

$$\epsilon_y = \frac{\epsilon_{XX}+\epsilon_{YY}}{2} - \frac{\epsilon_{XX}-\epsilon_{YY}}{2}\cos 2(\theta+180°) - \epsilon_{XY}\sin 2(\theta+180°). \quad (7)$$

For device structure, the axes system is defined as $x[\bar{1}10]$, $y[\bar{1}\bar{1}0]$, and $z[001]$ as shown in Fig. 2. The x and y axes are rotated by 135° about the Z axis from the XY axes position, suggesting $\theta=135°$ and the strain tensors for the real structure would be as follows:

$$\epsilon_x = \tfrac{1}{2}\epsilon_{XX} + \tfrac{1}{2}\epsilon_{YY} - \epsilon_{YY}, \quad (8)$$

$$\epsilon_y = \tfrac{1}{2}\epsilon_{XX} + \tfrac{1}{2}\epsilon_{YY} + \epsilon_{XY}, \quad (9)$$

$$\epsilon_z = \epsilon_Z. \quad (10)$$

Usually, the number of independent parameters to be determined can be reduced and this would facilitate the analysis of the CBED patterns. Two different types of strain phenomena: biaxial and uniaxial, will be discussed in the next section.

1. Biaxial strain analysis

When SiGe is grown epitaxially on the Si substrate, the Si atoms underneath are described as being subjected to biaxial tension and distorted tetragonally in the macroscopic framework.[7,15] Small microscopical strains in the lattice may exist depending on the distance from the stressors. The strain would incur changes in the tetrahedral angle in the planes both parallel (along $x[\bar{1}10]$ and $y[\bar{1}\bar{1}0]$ directions) and perpendicular (along $[001]$ direction) to the interface (see Fig. 2). Under the above condition, the same amount of distortion would be induced along the $X[100]$ and $Y[010]$ crystallographic directions and the angle γ depends on the coherence between the Si substrate and the SiGe layer.[7] For these, the following relations can be obtained (see Fig. 3):

$$a_X = a_Y \quad (11)$$

$$\frac{\Delta a_X}{a_{\mathrm{Si}}} = \frac{\Delta a_Y}{a_{\mathrm{Si}}} = -\frac{\Delta\gamma}{2}, \quad (12)$$

with $\Delta a_i = a_i - a_{\mathrm{Si}}$, $i=X,Y$. A further reduction in the number of independent parameters can be obtained by the following condition in which the orthogonality of the angles along the edges of the unit cell is preserved:[7]

$$\alpha = \beta = \frac{\pi}{2}. \quad (13)$$

Thus, under biaxial stress, the number of independent parameters can be reduced from six to two (a_X and a_Z).

2. Uniaxial strain analysis

Incorporation of the nitride capping film exerts a longitudinal mechanical compressive strain onto the gate electrode, hence creating a uniaxial strain channel along the $x[\bar{1}10]$ direction.[5,6] This would again generate the same amount of distortion along the $X[100]$ and $Y[010]$ crystallographic directions and Eqs. (11) and (12) still apply. To obtain the strain components for the device structure, Eqs. (8) and (9) can therefore be further simplified into

$$\epsilon_x = \epsilon_{XX} - \epsilon_{XY}, \quad (14)$$

$$\epsilon_y = \epsilon_{XX} + \epsilon_{XY}. \quad (15)$$

Additionally, under uniaxial stress conditions, planar strain approximation in which only strain in the $x-z$ plane is nonzero (see Fig. 2), is assumed and the following relation (see Fig. 4) can be derived:[9,16]

$$\alpha = \pi - \beta. \quad (16)$$

Subjected to the above conditions, the number of independent parameters to be determined can only be reduced from 6 to 3 (a_X, a_Z, and α). However, because of the constraint imposed by the planar strain approximation, the ε_y strain component which is in the $y[\bar{1}\bar{1}0]$ direction is assumed to be zero. For all the above strain analysis, a positive sign of the strain component is associated with a tensile strain and a negative sign with a compressive strain in the silicon substrate.

III. RESULTS AND DISCUSSIONS

A. Uniaxial stress case study: Overlay film stress

Figure 5 shows a cross-sectional bright field TEM image of a MOSFET with a stacked nitride overlay film. The five CBED measurement positions (numbered 1–5) from the source to the drain contacts are indicated and the CBED patterns are as shown in Fig. 5. The x axis is taken to be along the channel while the z axis is normal to the substrate surface. Distinct HOLZ line patterns were obtained at a distance of about 150 nm from the gate oxide/silicon substrate interface. Figure 6(a) compares the longitudinal ϵ_x strain variation of the Si_3N_4/SiO_xN_y and Si_3N_4 overlay nitride film samples, measured from the source to the drain contacts. For positions below the source and drain contacts (positions 1 and 5), the horizontal lattice strain of both samples depicts tensile characteristics ($\epsilon_x > 0$). This is attributed to the compressive overlying nitride film which exerts a tensile strain in the substrate underneath. However, at position 3, which is directly below the gate electrode, a compressive strain ($\epsilon_x < 0$) is observed. This agrees well with a previous study which asserted the phenomenon to the geometric effect in which the lattice strain below the gate electrode for a short-channel MOSFET was determined predominantly by the stress exerted onto the sidewall of the gate electrode by the nitride film.[2] Besides these, we can also see that the single stacked Si_3N_4 overlay film sample exhibited a larger spatial variation for the horizontal ϵ_x strain component when compared to the dual stacked Si_3N_4/SiO_xN_y film sample. Contrary to Fig. 6(a), the magnitude of the vertical ϵ_z strain component is opposite to that of ϵ_x as shown in Fig. 6(b).

Our strain results from CBED therefore suggest that the thin SiO_xN_y beneath the Si_3N_4 layer offers a cushioning ef-

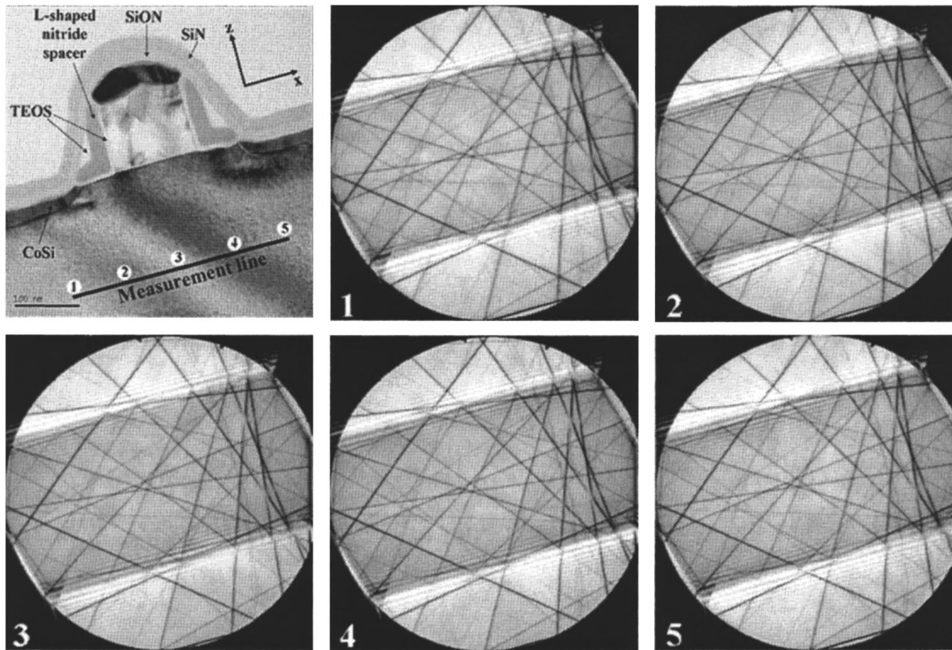

FIG. 5. Cross-sectional bright-field TEM image of an *n*-channel MOSFET with Si_3N_4/SiO_xN_y overlay nitride films. The CBED patterns, numbered 1–5, were taken from the measurement line marked on the bright-field image.

fect to the compressive stress induced by the Si_3N_4 overlay nitride film. Furthermore, these results obtained are in good agreement with the stress measurements obtained from the blanket wafers using the wafer bowing technique listed in Fig. 6(a). The relief in the compressive stress for the dual stacked sample can be rationalized by the more relaxed structural configuration of the SiO_xN_y in which the presence of the oxygen atom helps to add flexibility to the nitride film. As a consequence of the reduced compressive strain, it has further been shown in the electrical characterization that incorporating a thin layer of SiO_xN_y underneath the Si_3N_4 overlay film has resulted in an improvement in the electron mobility and drive current in *n*-channel MOSFETs but without much impact on the *p*-channel MOSFETs.

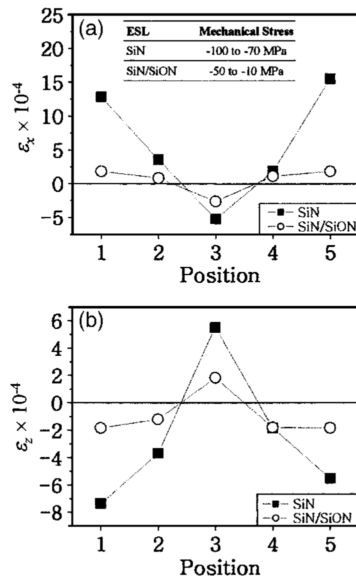

FIG. 6. (a) Lateral lattice strain ϵ_x, and (b) transverse lattice strain ε_z, obtained after simulation using JEMS software for Si_3N_4 and Si_3N_4/SiO_xN_y ESL samples measured from the CBED patterns taken from the Si substrate at positions marked by the numbers 1–5 in Fig. 5. The inset table in (a) shows the blanket film stress measurement for Si_3N_4 and Si_3N_4/SiO_xN_y films obtained by the wafer bowing method.

B. Biaxial stress case study: $Si_{1-x}Ge_x/Si$ heterostructures

Figure 7(a) depicts a sketch of the Ge profile in the graded layer for the two samples and Fig. 7(b) shows a high-angle annular dark-field (HAADF) TEM micrograph of the *G*1 sample. Twenty CBED images were captured from the measurement line as shown in the figure. The line was displaced

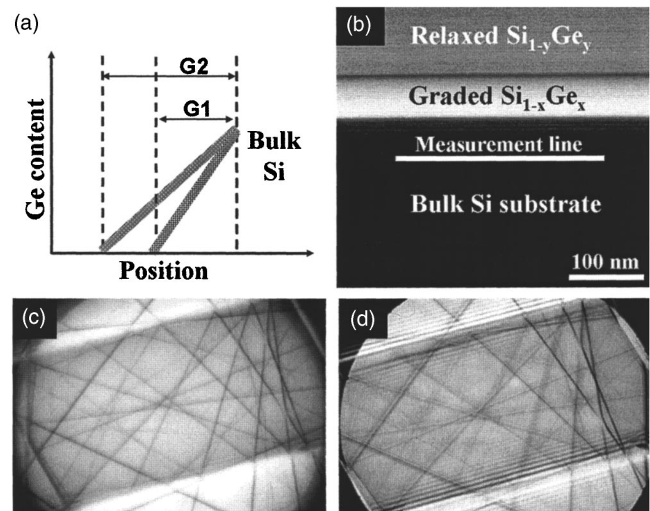

FIG. 7. (a) Sketch of the Ge profile in the graded layer for *G*1 and *G*2 samples. (b) HAADF TEM micrograph of the *G*1 sample. Examples of CBED patterns obtained for: (c) *G*1 and (d) *G*2 samples when the probe beam was placed at a distance of about 150 nm from the graded layer/bulk Si interface.

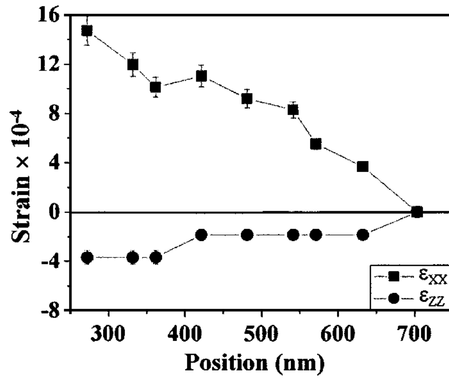

FIG. 8. Strain distribution for the components ϵ_{XX} and ϵ_{ZZ} in the Si substrate, obtained by CBED for sample $G1$. The position is the distance measured from the graded layer/bulk Si interface.

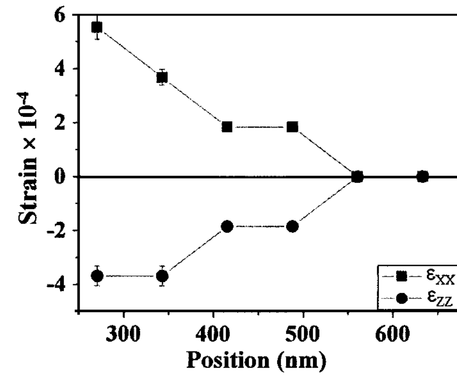

FIG. 9. Strain distribution for the components ϵ_{XX} and ϵ_{ZZ} in the Si substrate, obtained by CBED for sample $G2$. The position is the distance measured from the graded layer/bulk Si interface.

progressively at a small step away from the graded layer/bulk Si interface and detection was carried out continuously. When the measurement line was placed about 150 nm from the graded layer/bulk Si interface, distinct HOLZ patterns in which the stress is nearly constant within the probed area, can be obtained for sample $G1$ as shown in Fig. 7(c). However, when the probe beam was placed at the same distance away from the interface, HOLZ bands in which the HOLZ lines split into bands, were obtained for sample $G2$. An example of the CBED pattern of sample $G2$ obtained from the measurement line is depicted in Fig. 7(d). The above observation was related to the homogeneity of the analyzed volume near the interface. A poor quality diffraction pattern may be associated with a nanoregion consisting of different types of deformation (surface relaxation, strain field gradient, or geometry boundary effects of the dislocations) while a good quality diffraction pattern is attributed to a large homogeneously strained nanovolume of the crystal. This suggests that for $G2$, a greater amount of distortions are generated in the silicon lattice near the interface and this is probably related to the Ge compositional gradient in the graded layer. The CBED patterns obtained therefore provide an insight into the relaxation mechanism of the silicon lattice near the interface. Since the CBED technique is very sensitive to the localized behavior of the analyzed volume, a good signal obtained for the CBED patterns can be attributed to a region which is free of defects or steep field gradient.

Figures 8 and 9 show the ϵ_{XX} and ϵ_{ZZ} strain profiles obtained for $G1$ and $G2$, respectively, in the crystallographic orientations and the horizontal axis indicates the position of the electron probe beam from the graded layer/bulk Si substrate interface. For each sample, five diffraction patterns were simulated at a particular distance away from the interface. From both Figs. 8 and 9, we can see that $\varepsilon_{XX}>0$ and $\varepsilon_{ZZ}<0$. The observations obtained suggest that the silicon layer near the interface of the lattice-mismatched films was subjected to small local lattice distortion. Comparing the two samples, we can see that $G1$ depicts a larger ϵ_{XX} strain magnitude, suggesting that the silicon lattice is highly strained underneath the compositionally graded SiGe films. Furthermore, it requires a longer distance away from the graded layer/bulk Si substrate interface before the silicon lattice is completely undistorted. Based on the strain distribution profile obtained, sample $G1$ is associated with a steeper strain slope, which hence suggests that the lattice distortion obtained in the interfacial region is predominantly due to misfit dislocations rather than steep strain field gradient. In addition to these, for both $G1$ and $G2$ samples, we do not observe any significant variation for ϵ_{ZZ} strain along the [001] direction. Hence, the use of Poisson ratio, a macroscopic quantity, for understanding strain distribution, may not be applicable to the localized behavior of a few nanometer volume element.[17]

We suggest that the CBED results obtained for the two samples may be attributed to the minimum free energy criterion based on the theoretical predictions proposed by Matthews in which the total energy of a film material above its critical thickness is given by:[18–20]

$$E=E_{\epsilon}+E_{\delta}. \tag{17}$$

The first term is the elastic strain energy E_{ϵ} and the second term is the energy of the dislocation network E_{δ}. The energy of the heteroepitaxial systems aims to reach the minimum value at the thermodynamic equilibrium condition in which the lattice misfit f at the interface is accommodated between dislocations δ and strain ϵ in such a way that $f=\epsilon+\delta$.[21] In this case, elastic distortion seems to be more energetically favorable for sample $G1$ than for sample $G2$, which has a thicker graded layer and hence a more gentle compositional gradient. However, the exact explanation for the observations obtained need further investigation.

IV. CONCLUSIONS

In this article, we have outlined a detailed description of strain analysis using the CBED technique for advanced technological applications. We have shown that the methodology works on both the device structures and blanket wafers under uniaxial and biaxial stress, respectively. From the results, we can see that CBED measurements permit us to tailor the channel strain by making modifications to the capping layer of the MOSFETs and study the influence of compositional gradient of SiGe on the equilibrium structural condition of

the underlying Si substrate. Hence, the CBED technique, in conjunction with the implemented experimental procedure, could allow us to design high performance devices and look into the relaxation mechanism for heteroepitaxial systems with greater ease and efficiency.

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