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High spatial resolution mapping of strain induced by the geometry configuration in nanoscaled devices

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Mechanical stress effect induced by the geometry of the active region or the incorporation of different materials becomes an increasingly critical issue as the device dimensions continue to scale down.[1] Understanding stress-related performance issues requires the use of a strain measurement technique with high spatial resolution, especially when the device performance becomes affected by the local properties of the materials.[2] Convergent beam electron diffraction (CBED) has been used to measure local lattice parameters by detecting the shift in the high order Laue zone (HOLZ) lines. Nevertheless, a more accurate comparison between the experimental and modeling data is necessary so as to have a better understanding of the stresses built up by the different fabrication processes used for the silicon devices.[3,4] For previous CBED measurements of strain, only one-dimensional strain field plots are given and this does not explain the effect of the mechanical stress investigated. For this, a two-dimensional mapping of the strain field is essential.

In this work, we examine the influence of geometry configuration on the strain field distribution in the active regions of deep sub-micron silicon devices. Scanning transmission electron microscopy (STEM) mode coupled with high-angle annular dark-field (HAADF) detectors allows us to capture the diffraction patterns automatically. Strain analysis for the CBED patterns is carried out with JEMS software package of Stadelmann, this allows extraction of the local strain components of the deformed regions. Two different active region geometries are compared by the changing the active width: L=0.31 or 5 μm (as in Figure 1). In addition, modeling analysis and electrical characterization of the devices are also carried out. After which, the two-dimensional strain field maps, calculated strain distribution profiles and electrical characteristics are compared.

At a particular measurement distance from the interface, the lattice strain profiles obtained for L=0.31 μm is as shown in Figure 2. Nevertheless, the strain profiles are only one-dimensional representation of the strain field and would not completely elucidate the effect of the mechanical strain induced by the active geometry layout in the fabrication of the nanoscaled devices. Figure 3a shows the cross-sectional bright-field TEM image of the MOSFET with L=0.31 μm. A two dimensional mapping of the strain field is shown in Figure 3b, and from which, the strain propagation can be illustrated clearly and this can allow us to tailor the amount of strain in the channel region by modifying the surrounding features.

References

[1] A. Steegen and K. Maex, Mater. Sci. Eng., R. **38**, 1 (2002).
[2] A. Toda, N. Ikarashi, H. Ono, S. Ito, T. Toda, and K. Imai, Appl. Phys. Lett., **79**, 4243 (2001).
[3] A. Armigliato, R. Balboni, G.P. Carnevale, G. Pavia, D. Piccolo, S. Frabboni, A. Benedetti and A.G. Cullis, Appl. Phys. Lett., **82**, 2172 (2003).
[4] A. Armigliato, R. Balboni and S. Frabboni, Eur. Phys. J. Appl. Phys., **27**, 49 (2004).

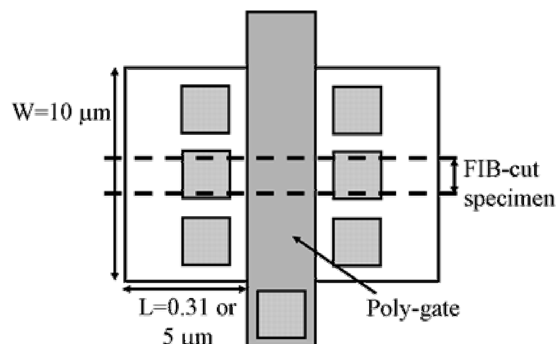

Fig. 1. Schematic layout of the MOSFET.

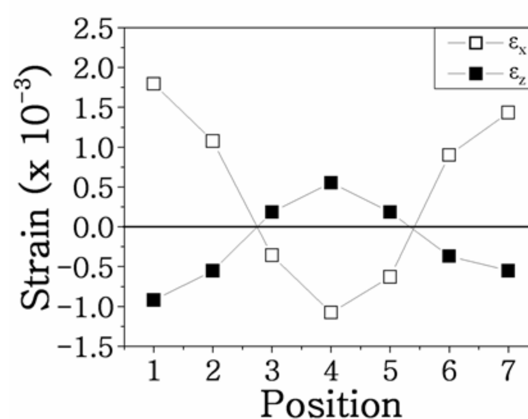

Fig. 2. One-dimensional lattice strain profiles obtained in the active region for MOSFET with (a) L=0.31 μm.

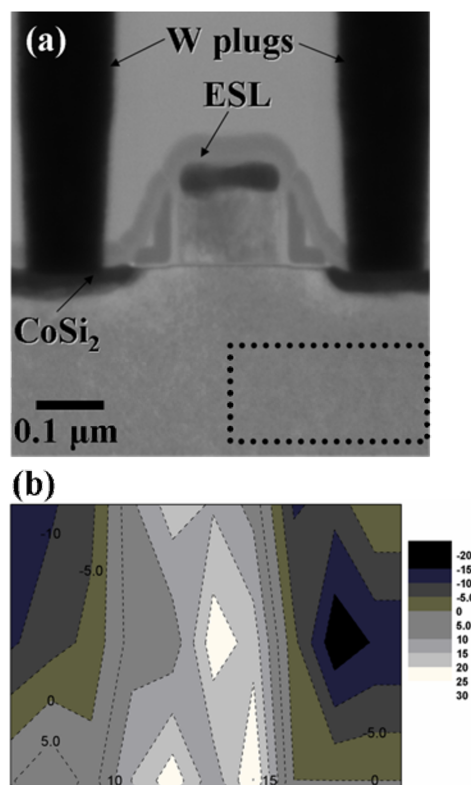

Fig. 3. (a) Cross-sectional bright-field TEM image of a MOSFET. (b) 2-dimensional strain map taken in the dotted region as shown in (a) for L=0.31 μm. Strain units are × 10^{-4}.